1M x 4BANKS x 16BITS SDRAM

Table of Content-

1. GENERAL DESCRIPTION

PT480416BG is a high-speed synchronous dynamic random access memory (SDRAM), organized as 1M words x 4 banks x 16 bits.

Accesses to the SDRAM are burst oriented. Consecutive memory location in one page can be accessed at a burst length of 1, 2, 4, 8 or full page when a bank and row is selected by an ACTIVE command. Column addresses are automatically generated by the SDRAM internal counter in burst operation. Random column read is also possible by providing its address at each clock cycle. The multiple bank nature enables interleaving among internal banks to hide the precharging time.

By having a programmable Mode Register, the system can change burst length, latency cycle, interleave or sequential burst to maximize its performance. PT480416BG is ideal for main memory in high performance applications.

2. FEATURES

- 3.3 /3.3±10% power supply
- 1048,576 words x 4 banks x 16 bits organization
- Self Refresh Current: Standard and Low Power
- CAS latency: 2 and 3
- Burst Length: 1, 2, 4, 8, and full page
- Sequential and Interleave burst
- Burst read, Single Write Operation
- Byte data controlled by DQM
- Power-down Mode
- Auto-precharge and controlled precharge
- 4K refresh cycles/64 mS
- Interface: LVTTL
- Packaged in VFBGA 60 balls pitch=0.65mm, using PB free with RoHS compliant.

3. PART NUMBER INFORMATION

PART NUMBER	SPEED (CL=3)	SELF REFRESH CURRENT (MAX.)
PT480416BG-6	166MHz	3mA
PT480416BG-7	143MHz	3mA

4. BALL CONFIGURATION

Top View

	1	2	6	7
A	VSS	DQ15	DQ0	VDD
B	DQ14	VSSQ	VDDQ	DQ1
C	DQ13	VDDQ	VSSQ	DQ2
D	DQ12	DQ11	DQ4	DQ3
E	DQ10	VSSQ	VDDQ	DQ5
F	DQ9	VDDQ	VSSQ	DQ6
G	DQ8	NC	NC	DQ7
H	NC	VSS	VDD	NC
J	NC	UDQM	LDQM	WE#
K	NC	CLK	RAS#	CAS#
L	CKE	NC	NC	CS#
M	A11	A9	BS1	BS0
N	A8	A7	A0	A10
P	A6	A5	A2	A1
R	VSS	A4	A3	VDD

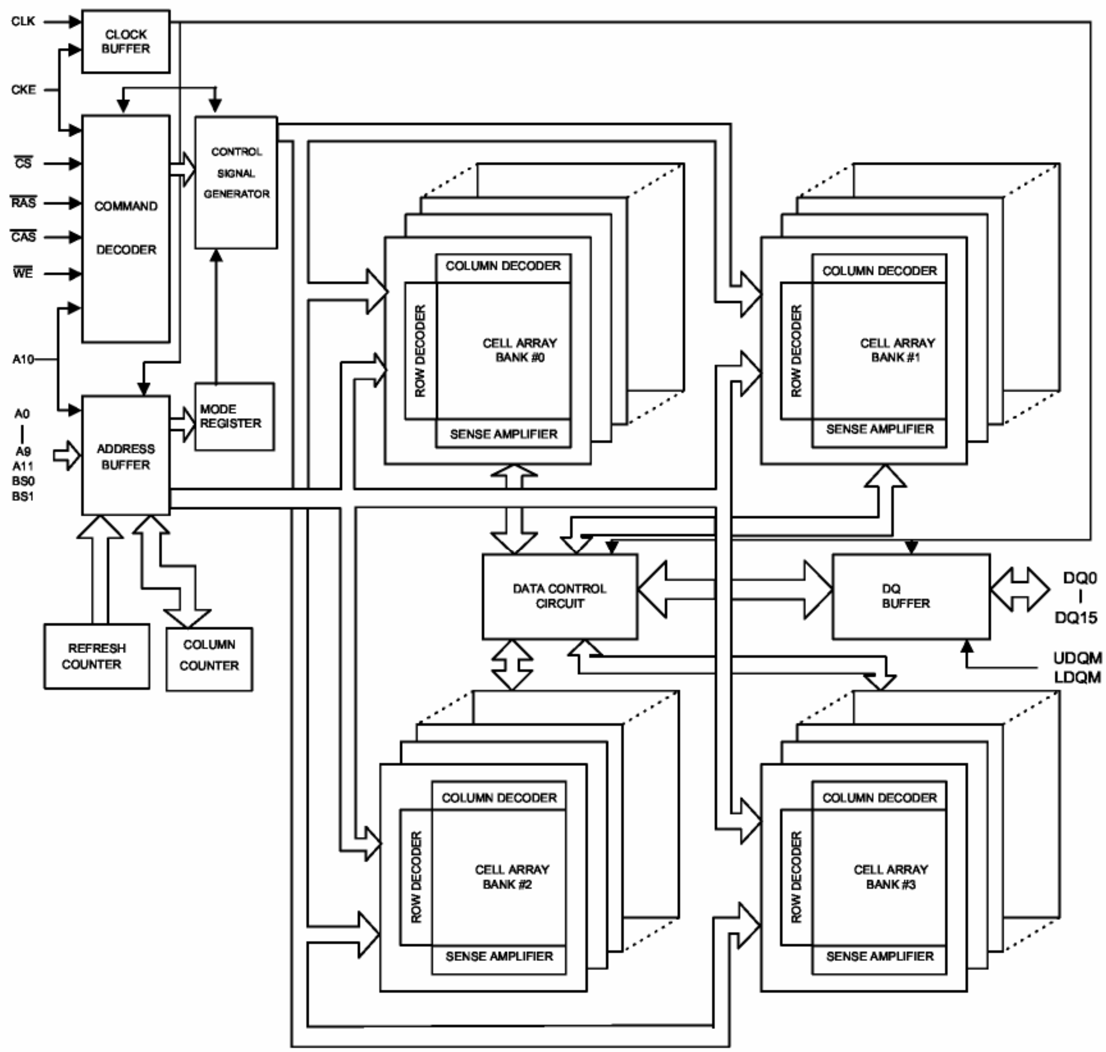
Bottom View

	7	6	2	1
A	VDD	DQ0	DQ15	VSS
B	DQ1	VDDQ	VSSQ	DQ14
C	DQ2	VSSQ	VDDQ	DQ13
D	DQ3	DQ4	DQ11	DQ12
E	DQ5	VDDQ	VSSQ	DQ10
F	DQ6	VSSQ	VDDQ	DQ9
G	DQ7	NC	NC	DQ8
H	NC	VDD	VSS	NC
J	WE#	LDQM	UDQM	NC
K	CAS#	RAS#	CLK	NC
L	CS#	NC	NC	CKE
M	BS0	BS1	A9	A11
N	A10	A0	A7	A8
P	A1	A2	A5	A6
R	VDD	A3	A4	VSS

5. BALL DESCRIPTION

BALL LOCATION	PIN NAME	FUNCTION	DESCRIPTION
M1,M2,N1,N2,N6, N7,P1,P2,P6,P7, R2,R6	A0－A11	Address	Multiplexed pins for row and column address. Row address: A0－A11. Column address: A0－A7.
M6,M7	BS0, BS1	Bank Select	Select bank to activate during row address latch time, or bank to read/write during address latch time.
A2,A6,B1,B7,C1,C7,D1,D2,D6,D7,E1,E7,F1,F7,G1,G7	DQ0-DQ15	Data Input/ Output	Multiplexed pins for data output and input.
L7	CS	Chip Select	Disable or enable the command decoder. When command decoder is disabled, new command is ignored and previous operation continues.
K6	RAS	Row Address Strobe	Command input. When sampled at the rising edge of the clock RAS, CAS and WE define the operation to be executed.
K7	CAS	Column Address Strobe	Referred to RAS
J7	WE	Write Enable	Referred to RAS
J2,J6	UDQM LDQM	Input/output mask	The output buffer is placed at Hi-Z (with latency of 2) when DQM is sampled high in read cycle. In write cycle, sampling DQM high will block the write operation with zero latency.
K2	CLK	Clock Inputs	System clock used to sample inputs on the rising edge of clock.
L1	CKE	Clock Enable	CKE controls the clock activation and deactivation. When CKE is low, Power Down mode, Suspend mode, or Self Refresh mode is entered.
A7,H6,R7	V_{DD}	Power (+3.3V)	Power for input buffers and logic circuit inside DRAM.
A1,H2,R1	V_{SS}	Ground	Ground for input buffers and logic circuit inside DRAM.
B6,C2,E6,F2	V_{DDQ}	Power (+3.3V) for I/O buffer	Separated power from V_{DD}, to improve DQ noise immunity.
B2,C6,E2,F6	V_{SSQ}	Ground for I/O buffer	Separated ground from V_{SS}, to improve DQ noise immunity.
G2,G6,H1,H7,J1, K1,L2,L6	NC	No Connection	No connection

6. BLOCK DIAGRAM



NOTE:
The cell array configuration is 4096 * 256 * 16

7. FUNCTIONAL DESCRIPTION

7.1 Power Up and Initialization

The default power up state of the mode register is unspecified. The following power up and initialization sequence need to be followed to guarantee the device being preconditioned to each user specific needs.

During power up, all V_{CC} and V_{CC}Q pins must be ramp up simultaneously to the specified voltage when the input signals are held in the "NOP" state. The power up voltage must not exceed V_{CC} +0.3V on any of the input pins or V_{CC} supplies. After power up, an initial pause of 200 μS is required followed by a precharge of all banks using the precharge command. To prevent data contention on the DQ bus during power up, it is required that the DQM and CKE pins be held high during the initial pause period. Once all banks have been precharged, the Mode Register Set Command must be issued to initialize the Mode Register. An additional eight Auto Refresh cycles (CBR) are also required before or after programming the Mode Register to ensure proper subsequent operation.

7.2 Programming Mode Register

After initial power up, the Mode Register Set Command must be issued for proper device operation. All banks must be in a precharged state and CKE must be high at least one cycle before the Mode Register Set Command can be issued. The Mode Register Set Command is activated by the low signals of RAS, CAS, CS and WE at the positive edge of the clock. The address input data during this cycle defines the parameters to be set as shown in the Mode Register Operation table. A new command may be issued following the mode register set command once a delay equal to t_{RSC} has elapsed. Please refer to the next page for Mode Register Set Cycle and Operation Table.

7.3 Bank Activate Command

The Bank Activate command must be applied before any Read or Write operation can be executed. The operation is similar to RAS activate in EDO DRAM. The delay from when the Bank Activate command is applied to when the first read or write operation can begin must not be less than the RAS to CAS delay time (t_{RCD}). Once a bank has been activated it must be precharged before another Bank Activate command can be issued to the same bank. The minimum time interval between successive Bank Activate commands to the same bank is determined by the RAS cycle time of the device (t_{RC}). The minimum time interval between interleaved Bank Activate commands (Bank A to Bank B and vice versa) is the Bank-to-Bank delay time (t_{RRD}). The maximum time that each bank can be held active is specified as t_{RAS}(max.).

7.4 Read and Write Access Modes

After a bank has been activated, a read or write cycle can be followed. This is accomplished by setting RAS high and CAS low at the clock rising edge after minimum of t_{RCD} delay. WE pin voltage level defines whether the access cycle is a read operation (WE high), or a write operation (WE low). The address inputs determine the starting column address. Reading or writing to a different row within an activated bank requires the bank be precharged and a new Bank Activate command be issued. When more than one bank is activated, interleaved bank Read or Write operations are possible. By using the programmed burst length and alternating the access and precharge operations between multiple banks, seamless data access operation among many different pages can be realized. Read or Write Commands can also be issued to the same bank or between active banks on every clock cycle.

7.5 Burst Read Command

The Burst Read command is initiated by applying logic low level to CS and CAS while holding RAS and WE high at the rising edge of the clock. The address inputs determine the starting column address for the burst. The Mode Register sets type of burst (sequential or interleave) and the burst length (1, 2, 4, 8, full page) during the Mode Register Set Up cycle.

7.6 Burst Write Command

The Burst Write command is initiated by applying logic low level to CS, CAS and WE while holding RAS high at the rising edge of the clock. The address inputs determine the starting column address. Data for the first burst write cycle must be applied on the DQ pins on the same clock cycle that the Write Command is issued. The remaining data inputs must be supplied on each subsequent rising clock edge until the burst length is completed. Data supplied to the DQ pins after burst finishes will be ignored.

7.7 Read Interrupted by a Read

A Burst Read may be interrupted by another Read Command. When the previous burst is interrupted, the remaining addresses are overridden by the new read address with the full burst length. The data from the first Read Command continues to appear on the outputs until the CAS latency from the interrupting Read Command the is satisfied.

7.8 Read Interrupted by a Write

To interrupt a burst read with a Write Command, DQM may be needed to place the DQs (output drivers) in a high impedance state to avoid data contention on the DQ bus. If a Read Command will issue data on the first and second clocks cycles of the write operation, DQM is needed to insure the DQs are tri-stated. After that point the Write Command will have control of the DQ bus and DQM masking is no longer needed.

7.9 Write Interrupted by a Write

A burst write may be interrupted before completion of the burst by another Write Command. When the previous burst is interrupted, the remaining addresses are overridden by the new address and data will be written into the device until the programmed burst length is satisfied.

7.10 Write Interrupted by a Read

A Read Command will interrupt a burst write operation on the same clock cycle that the Read Command is activated. The DQs must be in the high impedance state at least one cycle before the new read data appears on the outputs to avoid data contention. When the Read Command is activated, any residual data from the burst write cycle will be ignored.

7.11 Burst Stop Command

A Burst Stop Command may be used to terminate the existing burst operation but leave the bank open for future Read or Write Commands to the same page of the active bank, if the burst length is full page. Use of the Burst Stop Command during other burst length operations is illegal. The Burst Stop Command is defined by having RAS and CAS high with CS and WE low at the rising edge of the clock. The data DQs go to a high impedance state after a delay, which is equal to the CAS Latency in a burst read cycle, interrupted by Burst Stop. If a Burst Stop Command is issued during a full page burst write operation, then any residual data from the burst write cycle will be ignored.

7.12 Addressing Sequence of Burst Type

The disturb address is varied by the Burst Length as shown in Table.

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
				Type = Sequential	Type = Interleaved
2			**A0**		
			0	0-1	0-1
			1	1-0	1-0
4		**A1**	**A0**		
		0	0	0-1-2-3	0-1-2-3
		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
8	**A2**	**A1**	**A0**		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1 -2-3	4-5-6-7-0-1 -2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0

7.13 Auto-precharge Command

If A10 is set to high when the Read or Write Command is issued, then the auto-precharge function is entered. During auto-precharge, a Read Command will execute as normal with the exception that the active bank will begin to precharge automatically before all burst read cycles have been completed. Regardless of burst length, it will begin a certain number of clocks prior to the end of the scheduled burst cycle. The number of clocks is determined by CAS latency.

A Read or Write Command with auto-precharge can not be interrupted before the entire burst operation is completed. Therefore, using of a Read, Write, or Precharge Command is prohibited during a read or write cycle with auto-precharge. Once the precharge operation has started, the bank cannot be reactivated until the Precharge time (t_{RP}) has been satisfied. Issue of Auto-Precharge command is illegal if the burst is set to full page length. If A10 is high when a Write Command is issued, the Write with Auto-Precharge function is initiated. The SDRAM automatically enters the precharge operation two clock delay from the last burst write cycle. This delay is referred to as Write t_{WR}. The bank undergoing auto-precharge can not be reactivated until t_{WR} and t_{RP} are satisfied. This is referred to as t_{DAL}, Data-in to Active delay ($t_{DAL} = t_{WR} + t_{RP}$). When using the Auto-precharge Command, the interval between the Bank Activate Command and the beginning of the internal precharge operation must satisfy t_{RAS}(min).

7.14 Precharge Command

The Precharge Command is used to precharge or close a bank that has been activated. The Precharge Command is entered when CS, RAS and WE are low and CAS is high at the rising edge of the clock. The Precharge Command can be used to precharge each bank separately or all banks simultaneously. The address bits, A10, BS0 and BS1 are used to define which bank(s) is to be precharged when the command is issued. After the Precharge Command is issued, the precharged bank must be reactivated before a new read or write access can be executed. The delay between the Precharge Command and the Activate Command must be greater than or equal to the Precharge time (t_{RP}).

7.15 Self Refresh Command

The Self-Refresh Command is defined by having CS, RAS, CAS and CKE held low with WE high at the rising edge of the clock. All banks must be idle prior to issuing the Self-Refresh Command. Once the command is registered, CKE must be held low to keep the device in Self-Refresh mode. When the SDRAM has entered Self Refresh mode all of the external control signals, except CKE, are disabled. The clock is internally disabled during Self-Refresh Operation to save power. The device will exit Self-Refresh operation after CKE is returned high. Any subsequent commands can be issued after t_{RC} from the end of Self Refresh command.

If, during normal operation, Auto-Refresh cycles are issued in bursts (as opposed to being evenly distributed), a burst of 4,096 Auto-Refresh cycles should be completed just prior to entering and just after exiting the Self-Refresh mode.

7.16 Power Down Mode

The Power Down mode is initiated by holding CKE low. All of the receiver circuits except CKE are gated off to reduce the power. The Power Down mode does not perform any refresh operations; therefore the device can not remain in Power Down mode longer than the Refresh period (t_{REF}) of the device.

The Power Down mode is exited by bringing CKE high. When CKE goes high, a No Operation Command is required on the next rising clock edge, depending on t_{CK}. The input buffers need to be enabled with CKE held high for a period equal to t_{CKS}(min) + t_{CK}(min).

7.17 No Operation Command

The No Operation Command should be used in cases when the SDRAM is in an idle or a wait state to prevent the SDRAM from registering any unwanted commands between operations. A No Operation Command is registered when CS is low with RAS, CAS, and WE held high at the rising edge of the clock. A No Operation Command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

7.18 Deselect Command

The Deselect Command performs the same function as a No Operation Command. Deselect Command occurs when CS is brought high, the RAS, CAS, and WE signals become don't cares.

7.19 Clock Suspend Mode

During normal access mode, CKE must be held high enabling the clock. When CKE is registered low while at least one of the banks is active, Clock Suspend Mode is entered. The Clock Suspend mode deactivates the internal clock and suspends any clocked operation that was currently being executed. There is a one-clock delay between the registration of CKE low and the time at which the SDRAM operation suspends. While in Clock Suspend mode, the SDRAM ignores any new commands that are issued. The Clock Suspend mode is exited by bringing CKE high. There is a one-clock cycle delay from when CKE returns high to when Clock Suspend mode is exited.

8. TABLE OF OPERATING MODES

Fully synchronous operations are performed to latch the commands at the positive edges of CLK. Table 1 shows the truth table for the operation commands.

TABLE 1 TRUTH TABLE (NOTE 1, 2)

COMMAND	DEVICE STATE	CKEN-1	CKEN	DQM	BS0,1	A10	A9-0 A11	CS	RAS	CAS	WE
Bank Active	Idle	H	X	X	V	V	V	L	L	H	H
Bank Precharge	Any	H	X	X	V	L	X	L	L	H	L
Precharge All	Any	H	X	X	X	H	X	L	L	H	L
Write	Active(3)	H	X	X	V	L	V	L	H	L	L
Write with Autoprecharge	Active(3)	H	X	X	V	H	V	L	H	L	L
Read	Active(3)	H	X	X	V	L	V	L	H	L	H
Read with Autoprecharge	Active(3)	H	X	X	V	H	V	L	H	L	H
Mode Register Set	Idle	H	X	X	V	V	V	L	L	L	L
No-Operation	Any	H	X	X	X	X	X	L	H	H	H
Burst Stop	Active (4)	H	X	X	X	X	X	L	H	H	L
Device Deselect	Any	H	X	X	X	X	X	H	X	X	X
Auto-Refresh	Idle	H	H	X	X	X	X	L	L	L	H
Self-Refresh Entry	Idle	H	L	X	X	X	X	L	L	L	H
Self-Refresh Exit	Idle (S.R)	L L	H H	X X	X X	X X	X X	H L	X H	X H	X X
Clock Suspend Mode Entry	Active	H	L	X	X	X	X	X	X	X	X
Power Down Mode Entry	Idle Active (5)	H H	L L	X X	X X	X X	X X	H L	X H	X H	X X
Clock Suspend Mode Exit	Active	L	H	X	X	X	X	X	X	X	X
Power Down Mode Exit	Any (Power down)	L L	H H	X X	X X	X X	X X	H L	X H	X H	X X
Data Write/Output Enable	Active	H	X	L	X	X	X	X	X	X	X
Data Write/Output Disable	Active	H	X	H	X	X	X	X	X	X	X

Notes:

(1) V = Valid, X = Don't care, L = Low Level, H = High Level

(2) CKEn signal is input level when commands are provided.

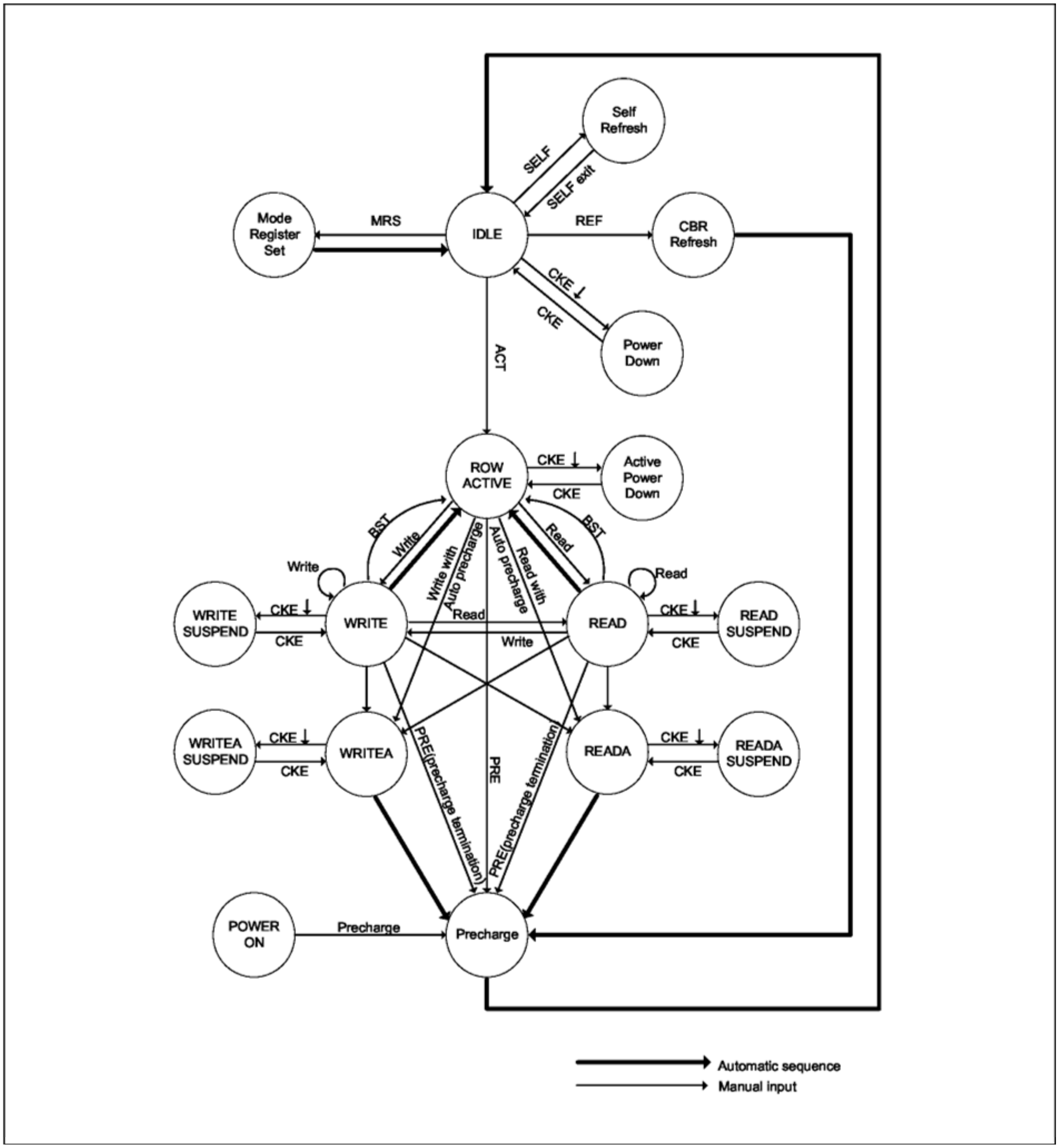
(3) These are state of bank designated by BS0,BS1 signals.

(4) Device state is full page burst operation.

(5) Power Down Mode can not be entered in the burst cycle.

When this command asserts in the burst cycle, device state is clock suspend mode.

8.1 Simplified State Diagram



Notes:

MRS = Mode Register Set
REF = Refresh
ACT = Active
PRE = Precharge
WRITEA = Write with Auto Precharge
READA = Read with Auto Precharge

9. ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTES
Input, Output Voltage	V_{IN}, V_{OUT}	-0.3—V_{CC}+0.3	V	1
Power Supply Voltage	V_{CC}, $V_{CC}Q$	-0.3—4.6	V	1
Operating Temperature	T_{OPR}	0—70	°C	1
Storage Temperature	T_{STG}	-55—150	°C	1
Soldering Temperature (10s)	T_{SOLDER}	260	°C	1
Power Dissipation	P_D	1	W	1
Short Circuit Output Current	I_{OUT}	50	mA	1

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

10. RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0 to 70℃)

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	NOTES
Power Supply Voltage	V_{CC}	3.0	3.3	3.6	V	2
Power Supply Voltage (for I/O Buffer)	$V_{CC}Q$	3.0	3.3	3.6	V	2
Input High Voltage	V_{IH}	2.0	-	V_{CC} +0.3	V	2
Input Low Voltage	V_{IL}	-0.3	-	0.8	V	2

Note: VIH (max.) = VCC/VCCQ +1 .2V for pulse width < 5 nS

VIL (min.) = VSS/VSSQ -1 .2V for pulse width < 5 nS

11 CAPACITANCE

(V_{CC} = 2.7V~3.6V, T_A = 25 C, f = 1MHz)

PARAMETER	SYM.	MIN.	MAX.	UNIT
Input Capacitance (A0 to A11, BS0,BS1, CS , RAS , CAS , WE, DQM, CKE)	C_{I1}	2.5	4	p f
Input Capacitance (CLK)	C_{CLK}	2.5	4	pf
Input/Output capacitance (DQ0 to DQ15)	C_{IO}	4	6.5	pf

Note: These parameters are periodically sampled and not 100% tested

12. DC CHARACTERISTICS

(V_{CC} = 3.3V ±0.3V, T_A = 0°~70°C)

PARAMETER		SYM.	-6 MAX.	-7 MAX.	UNIT	NOTES
Operating Current tCK = min., tRC = min. Active precharge command cycling without burst operation	1 bank operation	ICC1	90	80		3
Standby Current t_{CK} = min., CS = V_{IH} $V_{IH/L}$ = V_{IH} (min.) /V_{IL} (max.) Bank: inactive state	CKE = V_{IH}	ICC2	35	30		3
	CKE = V_{IL} (Power down mode)	ICC2P	3	3		3
Standby Current CLK = V_{IL}, CS = V_{IH} $V_{IH/L}$ = V_{IH} (min.) /V_{IL} (max.) Bank: inactive state	CKE = V_{IH}	ICC2S	8	8		
	CKE = V_{IL} (Power down mode)	ICC2PS	3	3	mA	
No Operating Current t_{CK} = min., CS = V_{IH} (min.) Bank: active state (2 banks)	CKE = V_{IH}	ICC3	60	55		
	CKE = V_{IL} (Power Down mode)	ICC3P	15	15		
Burst Operating Current Read/ Write command cycling	(t_{CK} = min.)	ICC4	165	145		3, 4
Auto Refresh Current Auto refresh command cycling	(t_{CK} = min.)	ICC5	120	110		3
Self Refresh Current (CKE = 0.2V) Self refresh mode	Standard	ICC6	3	3	mA	

PARAMETER	SYM.	MIN.	MAX.	UNIT	NOTES
Input Leakage Current (0V≦V_{IN}≦V_{CC}, all other pins not under test = 0V)	$I_{I(L)}$	-5	5	μA	
Output Leakage Current (Output disable , 0V≦V_{OUT} ≦V_{CC}Q)	$I_{O(L)}$	-5	5	μA	
LVTTL Output "H" Level Voltage (I_{OUT} = -2 mA)	V_{OH}	2.4	-	V	
LVTTL Output "L" Level Voltage (I_{OUT} = 2 mA)	V_{OL}	-	0.4	V	

13. AC CHARACTERISTICS

(V_{CC} = 3.3V±0.3V, V_{SS} = 0V, T_A = 0 to 70℃, Notes: 5, 6, 7, 8)

PARAMETER	SYM.	-6		-7		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.		
Ref/Active to Ref/Active Command Period	t_{RC}	60		65		nS	
Active to Precharge Command Period	t_{RAS}	42	100000	45	100000		
Active to Read/Write Command Delay Time	t_{RCD}	18		20			
Read/Write(a) to Read/Write(b) Command Period	t_{CCD}	1		1		t_{CK}	
Precharge to Active(b) Command Period	t_{RP}	18		20		nS	
Active(a) to Active(b) Command Period	t_{RPD}	12		14			
Write Recovery Time	t_{WR}	2		2		t_{CK}	
		2		2			
CLK Cycle Time	t_{CK}	10	1000	10	1000	nS	
		6	1000	7	1000		
CLK High Level Width	t_{CH}	2		2			
CLK Low Level Width	t_{CL}	2		2			
Access Time from CLK	t_{AC}		6		6		
			5		5.5		
Output Data Hold Time	t_{OH}	2		2			
Output Data High Impedance Time	t_{HZ}	2	6	2	7		
Output Data Low Impedance Time	t_{LZ}	0		0			
Power Down Mode Entry Time	t_{SB}	0	6	0	7		
Transition Time of CLK (Rise and Fall)	t_T	0.5	1	0.5	1		
Data-in-Set-up Time	t_{DS}	1.5		1.5			
Data-in Hold Time	t_{DH}	0.7		1			
Address Set-up Time	t_{AS}	1.5		1.5			
Address Hold Time	t_{AH}	0.7		1			
CKE Set-up Time	t_{CKS}	1.5		1.5			
CKE Hold Time	t_{CKH}	0.7		1			
Command Set-up Time	t_{CMS}	1.5		1.5			
Command Hold Time	t_{CMH}	0.8		1			
Refresh Time	t_{REF}		64		64	mS	
Mode Register Set Cycle Time	t_{RSC}	12		14		nS	

(L):For low power

Notes:

(1) Operation exceeds "ABSOLUTE MAXIMUM RATING" may cause permanent damage to the devices.

(2) All voltages are referenced to VSS

(3) These parameters depend on the cycle rate and listed values are measured at a cycle rate with the minimum values of tCK and tRC.

(4) These parameters depend on the output loading conditions. Specified values are obtained with output open.

(5) Power up sequence

(1) Power up must be performed in the following sequence.

(2) Power must be applied to VCC and VCCQ (simultaneously) while all input signals are held in the "NOP" state. The CLK signals must be started at the same time.

(3) After power-up a pause of at least 200 μseconds is required. It is required that DQM and CKE signals then be held " high" (VCC levels) to ensure that the DQ output is impedance.

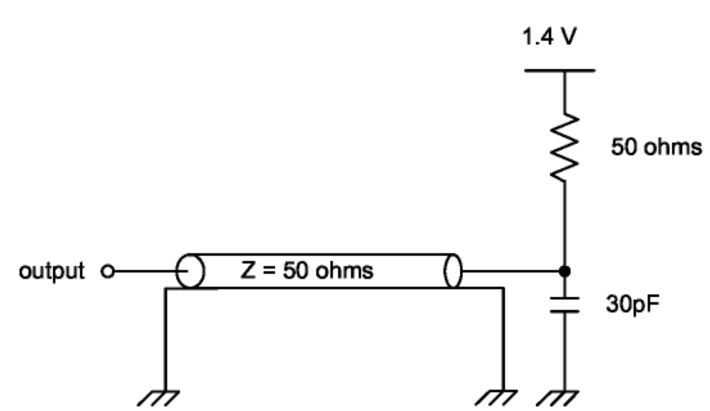
(4) All banks must be precharged.

(5) The Mode Register Set command must be asserted to initialize the Mode Register.

(6) A minimum of eight Auto Refresh dummy cycles is required to stabilize the internal circuitry of the device.

(6) AC test conditions.

PARAMETER	CONDITIONS
Output Reference Level	1.4V/1.4V
Output Load	See diagram below
Input Signal Levels	2.4V/0.4V
Transition Time (Rise and Fall) of Input Signal	2 nS
Input Reference Level	1.4V



AC TEST LOAD

1. Transition times are measured between VIH and VIL.
2. Thz defines the time at which the outputs achieve the open circuit condition and is not referenced to output level.
3. These parameters account for the number of clock cycles and depend on the operating frequency of the clock, as follows the number of clock cycles = specified value of timing/ clock period
   (count fractions as whole number)

(1) Tch is the pulse width of CLK measured from the positive edge to the negative edge referenced to VIH (min.).

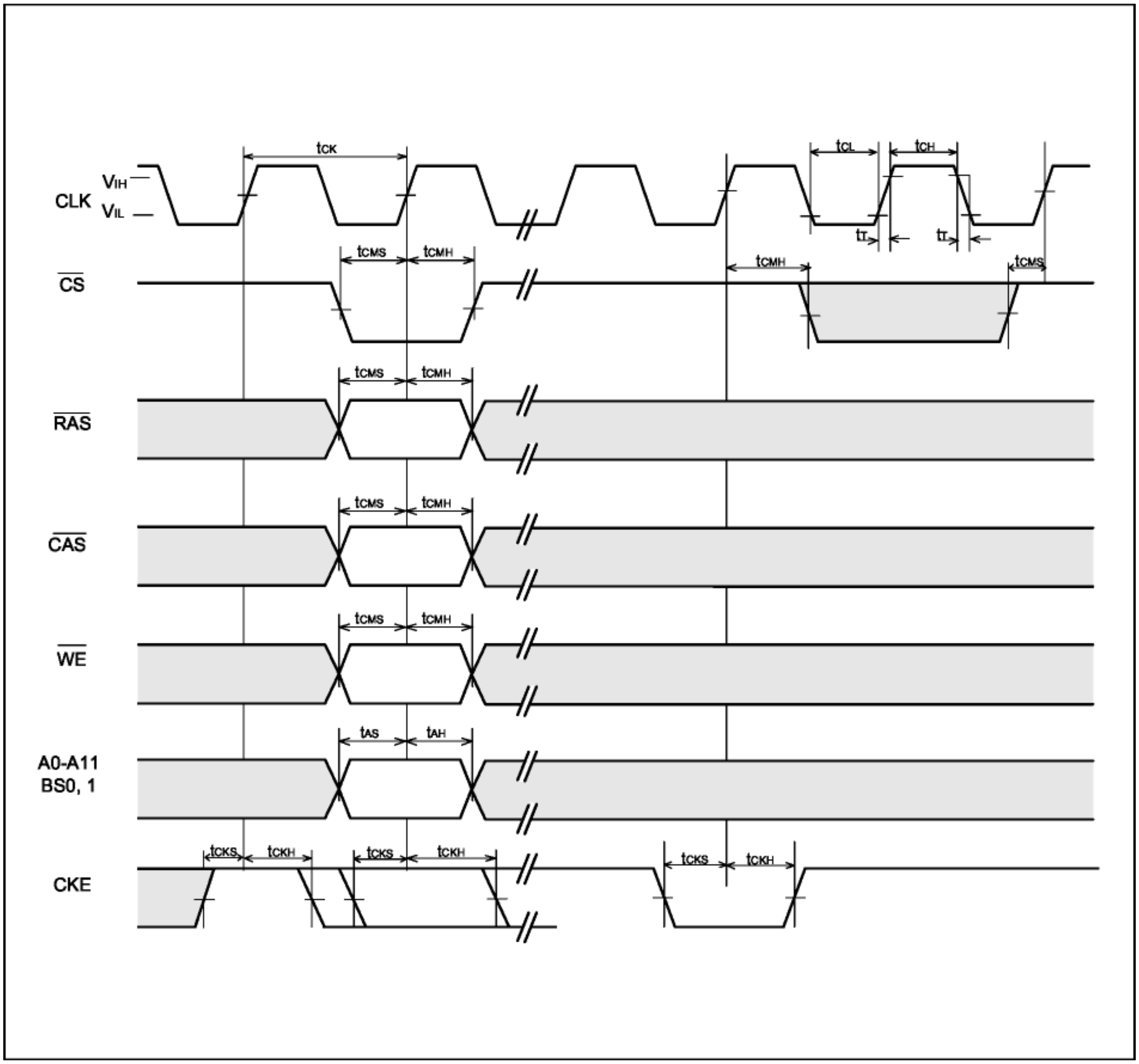
Tcl is the pulse width of CLK measured from the negative edge to the positive edge referenced to VIL (max.)

(2) AC Latency Characteristics

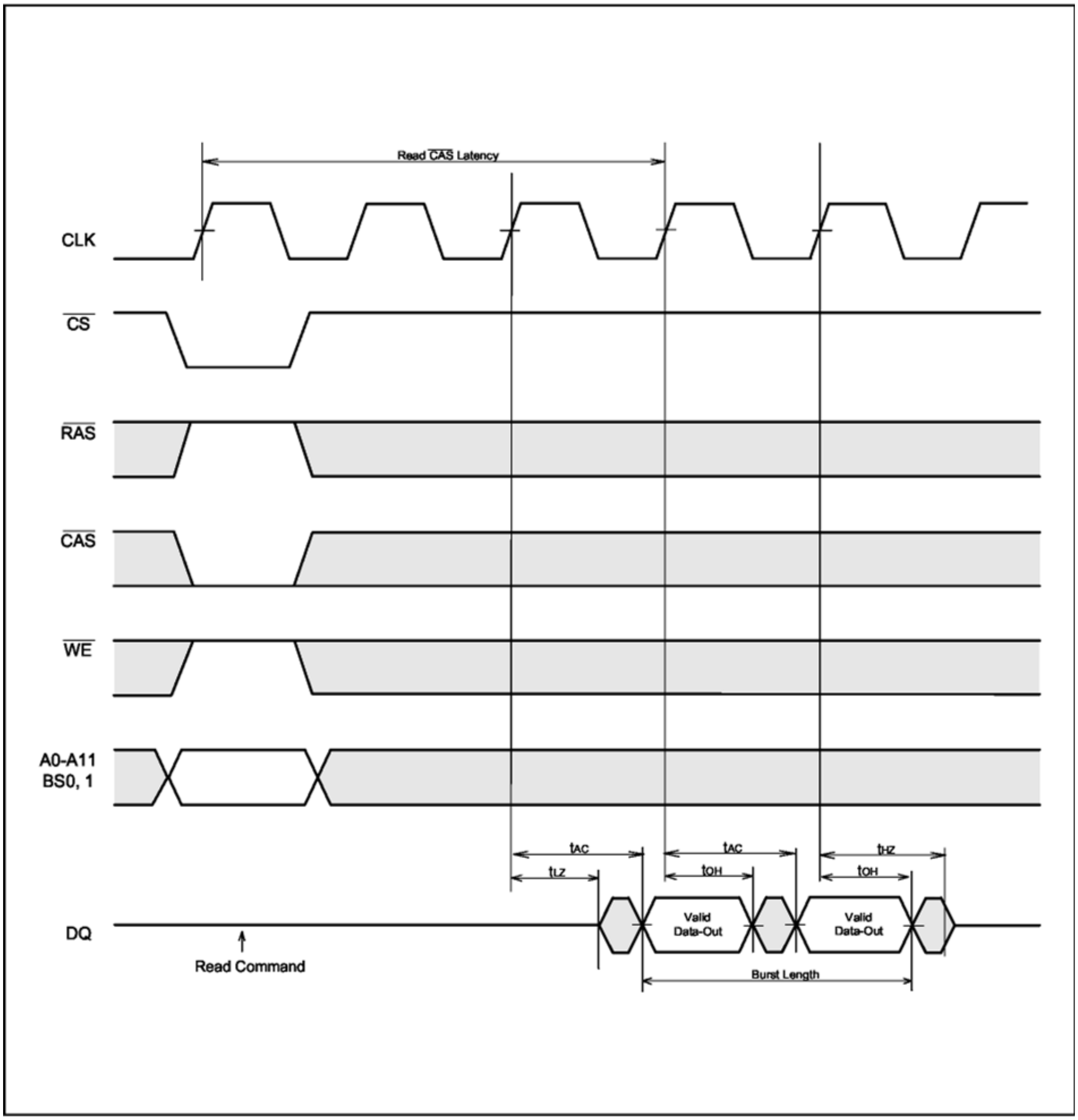
CKE to clock disable (CKE Latency)		1	tCK
DQM to output to HI-Z (Read DQM Latency)		2	
DQM to output to HI-Z (Write DQM Latency)		0	
Write command to input data (Write Data Latency)		0	
CS to Command input (CS Latency)		0	
Precharge to DQ Hi-Z Lead time	CL = 2	2	
	CL = 3	3	
Precharge to Last Valid data out	CL = 2	1	
	CL = 3	2	
Bust Stop Command to DQ Hi-Z Lead time	CL = 2	2	
	CL = 3	3	
Bust Stop Command to Last Valid Data out	CL = 2	1	
	CL = 3	2	
Read with Auto-precharge Command to Active/Ref Command	CL = 2	BL + tRP	tCK + nS
	CL = 3	BL + tRP	
Write with Auto-precharge Command to Active/Ref Command	CL = 2	(BL+1) + tRP	
	CL = 3	(BL+1) + tRP	

14. TIMING WAVEFORMS

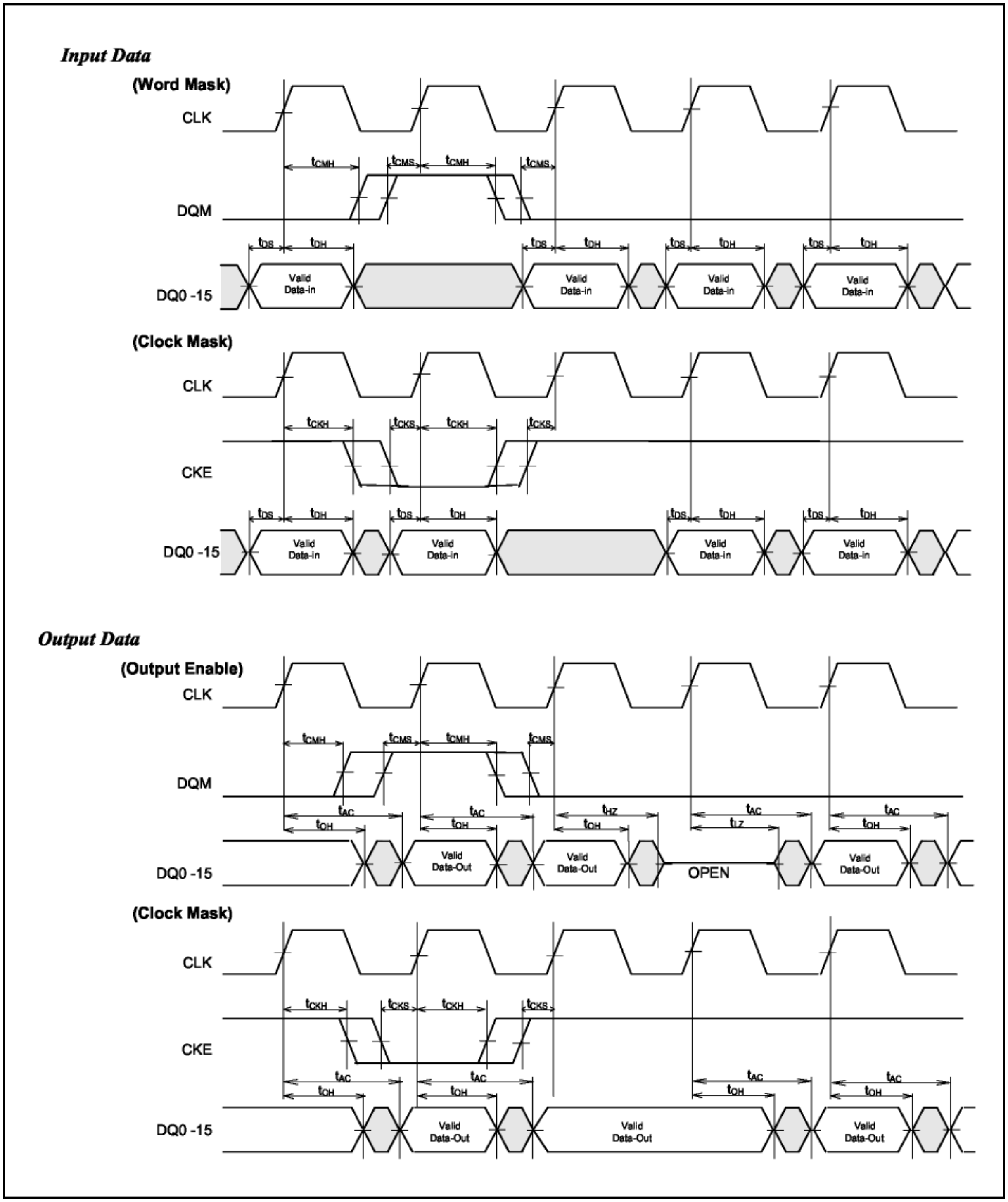
14.1 Command Input Timing



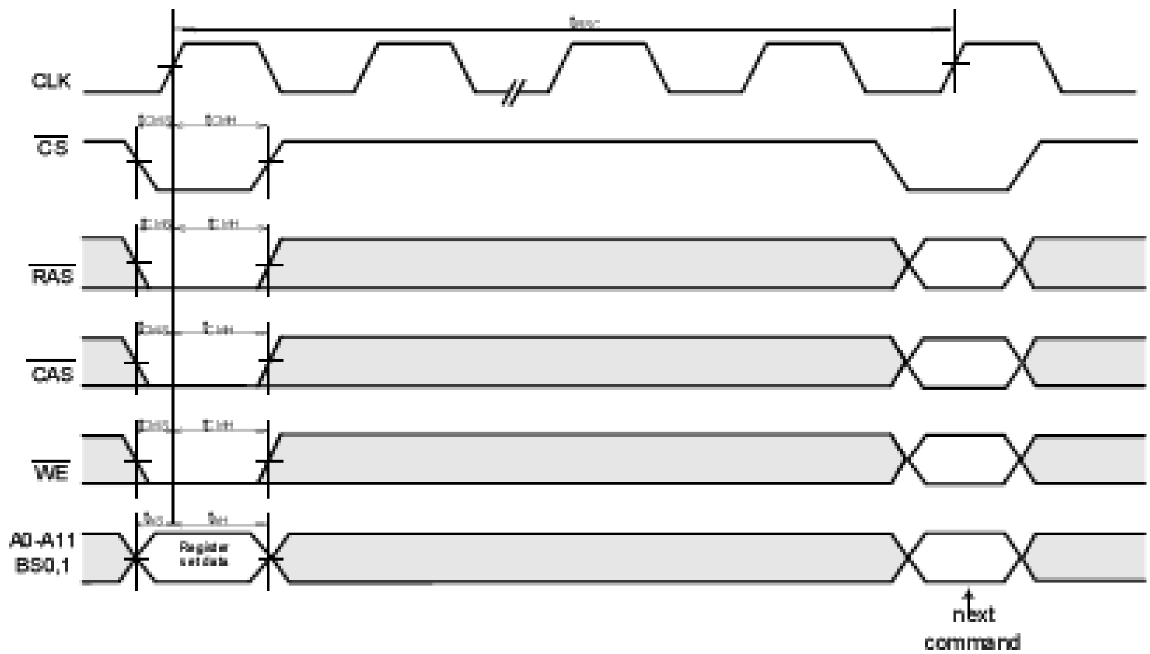
14.2 Read Timing



14.3 Control Timing of Input/Output Data



14.4 Mode Register Set Cycle



Address		
A0	Burst Length	
A1	Burst Length	
A2	Burst Length	
A3	Addressing Mode	
A4	CAS Latency	
A5	CAS Latency	
A6	CAS Latency	
A7	"0"	(Test Mode)
A8	"0"	Reserved
A9	Write Mode	
A10	"0"	Reserved
A11	"0"	Reserved
BS0	"0"	Reserved
BS1	"0"	Reserved

A2	A1	A0	Burst Length Sequential	Burst Length Interleave
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Full Page	Reserved

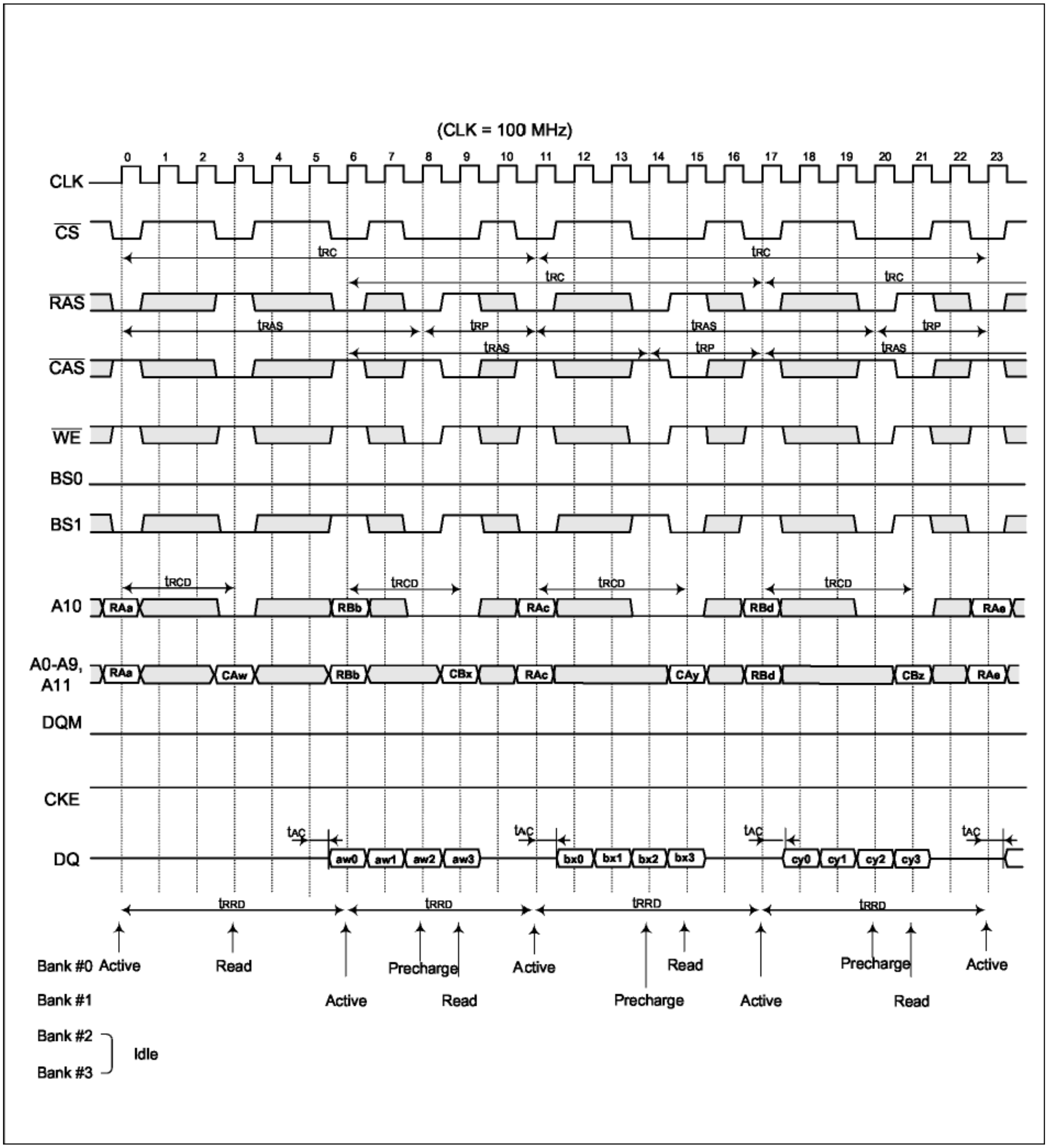
A3	Addressing Mode
0	Sequential
1	Interleave

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved

A9	Single Write Mode
0	Burst read and Burst write
1	Burst read and single write

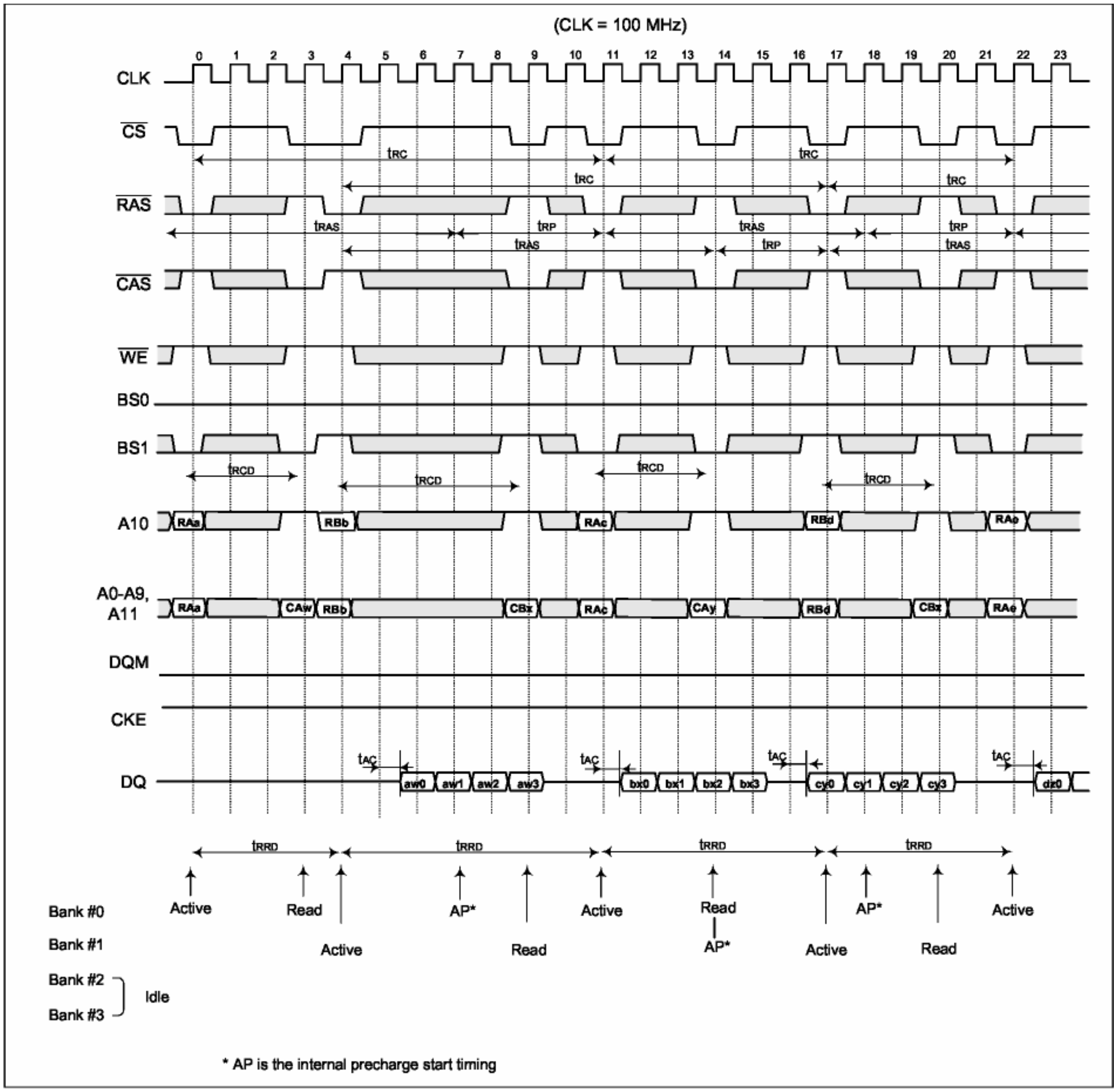
14.5 Interleaved Bank Read

(Burst Length = 4, CAS Latency = 3)



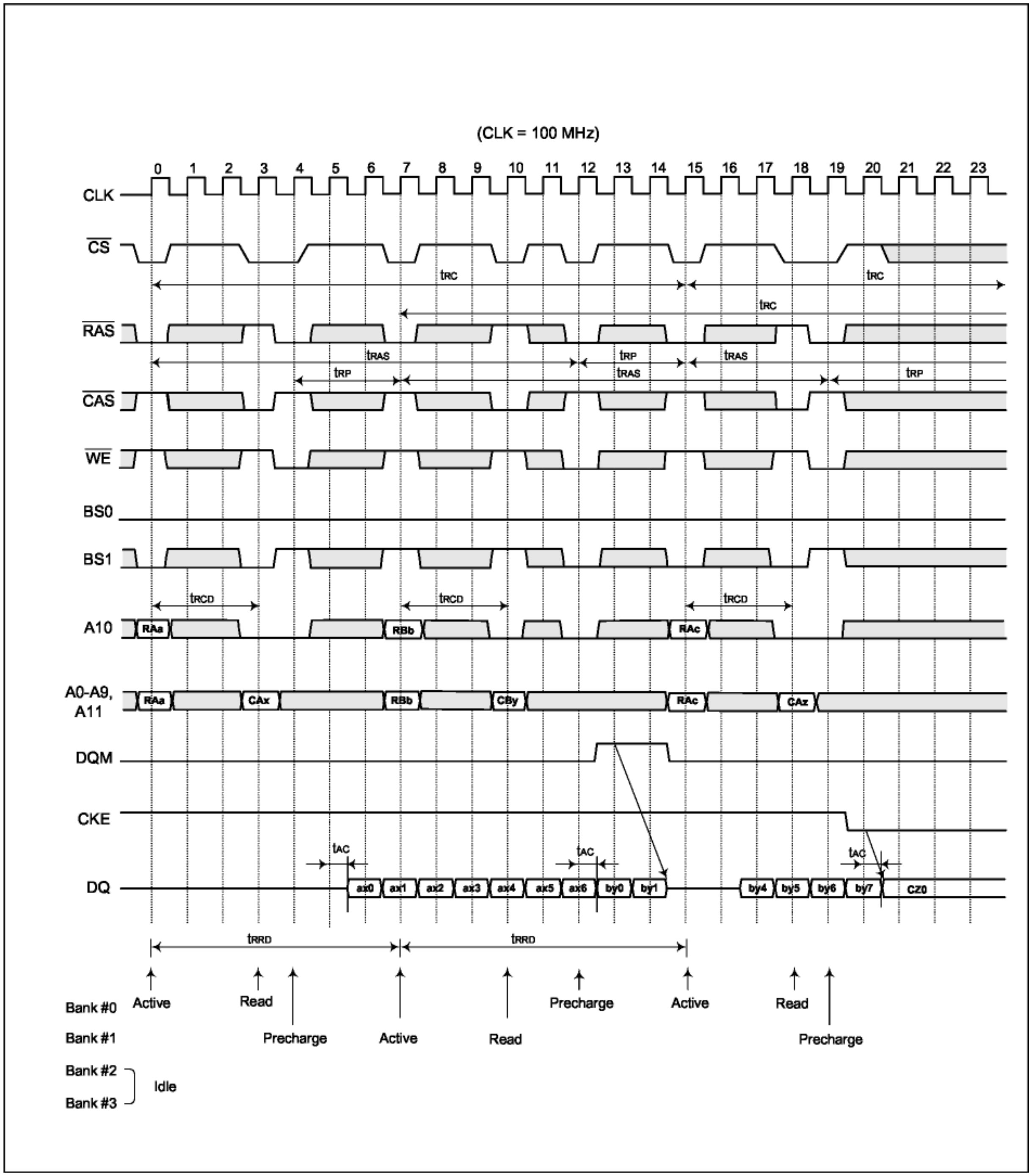
14.6 Interleaved Bank Read

(Burst Length = 4, CAS Latency = 3, Autoprecharge)



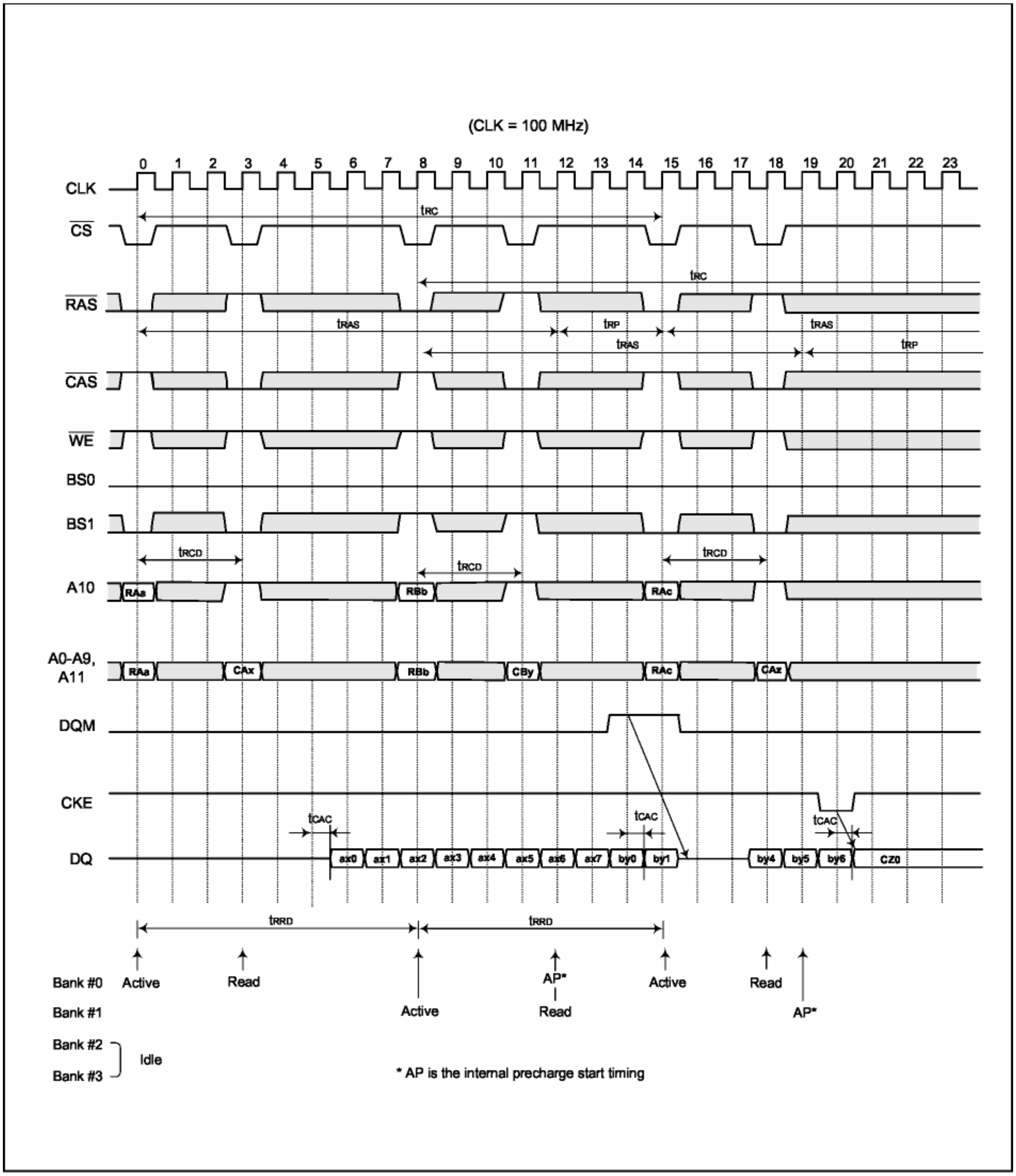
14.7 Interleaved Bank Read

(Burst Length = 8, CAS Latency = 3)



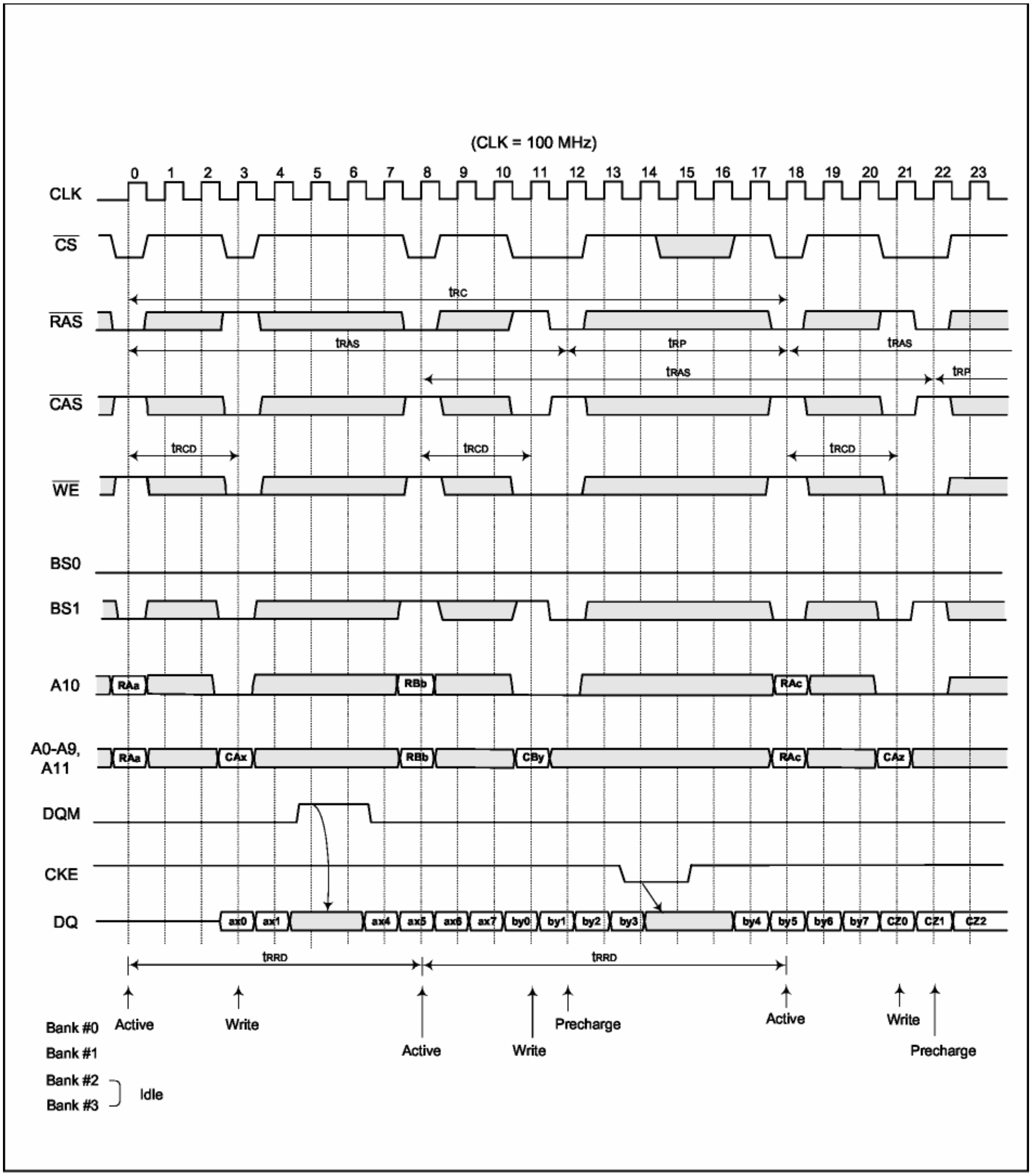
14.8 Interleaved Bank Read

(Burst Length = 8, CAS Latency = 3, Autoprecharge)



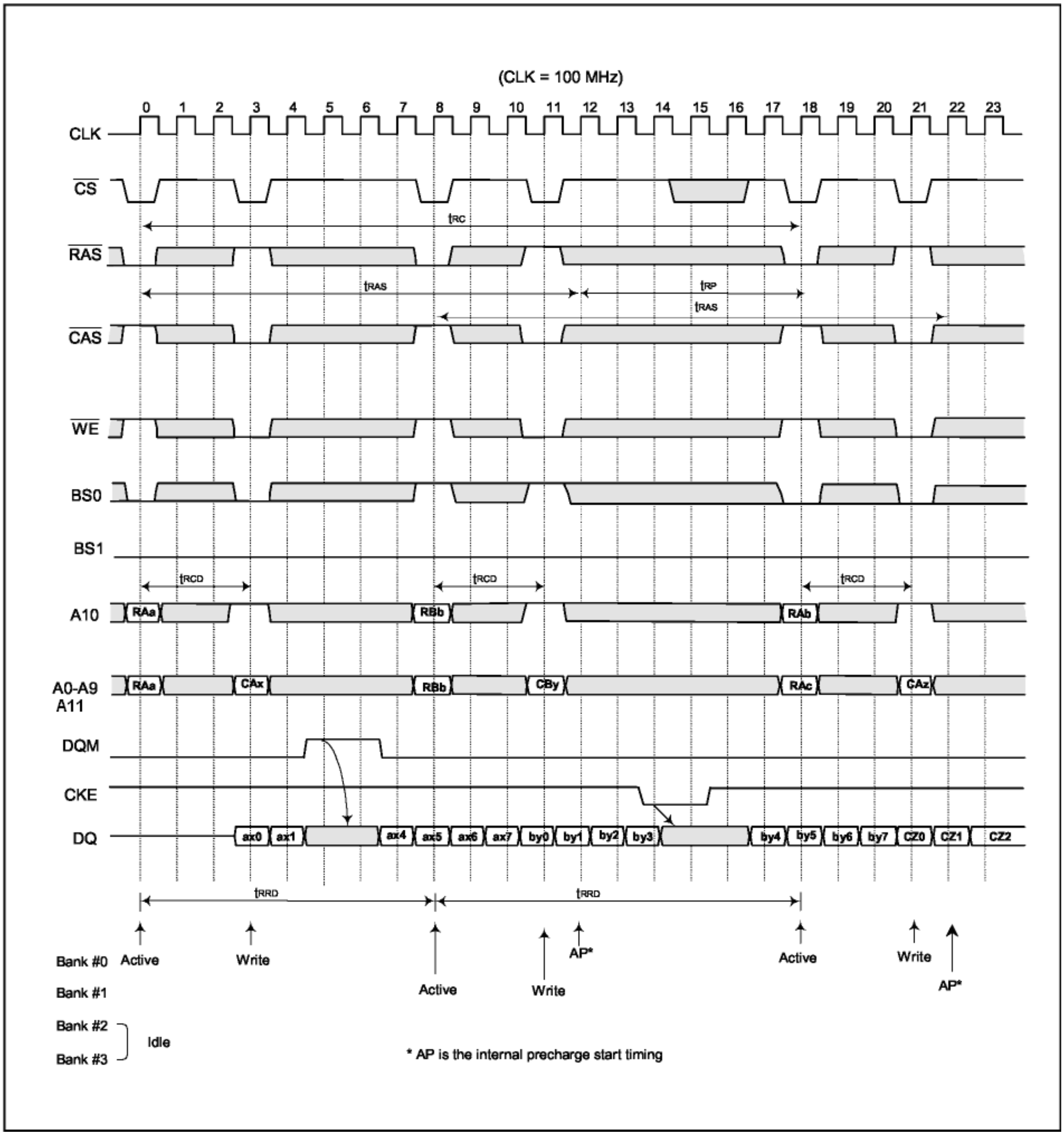
14.9 Interleaved Bank Write

(Burst Length = 8)



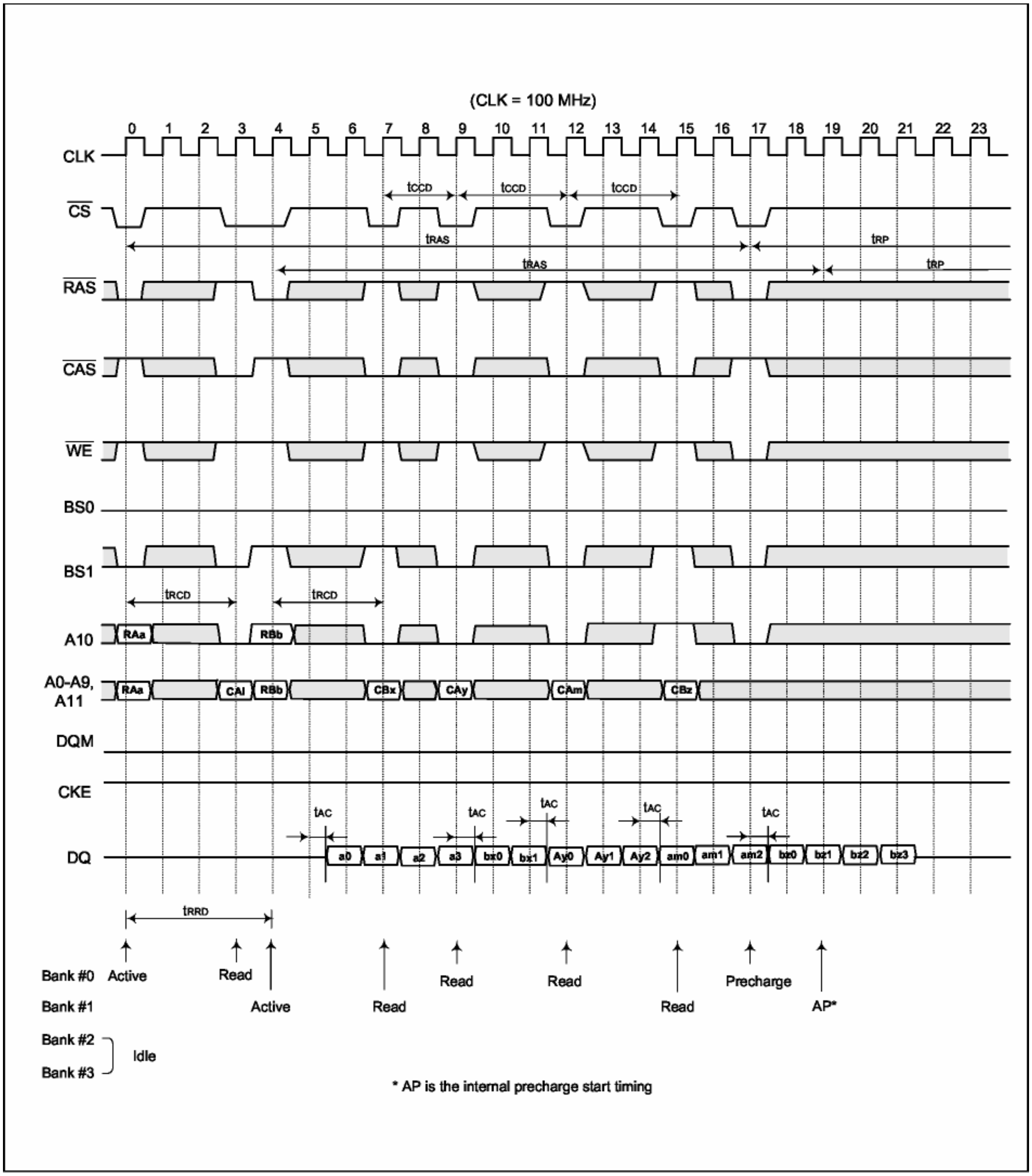
14.10 Interleaved Bank Write

(Burst Length = 8, Autoprecharge)



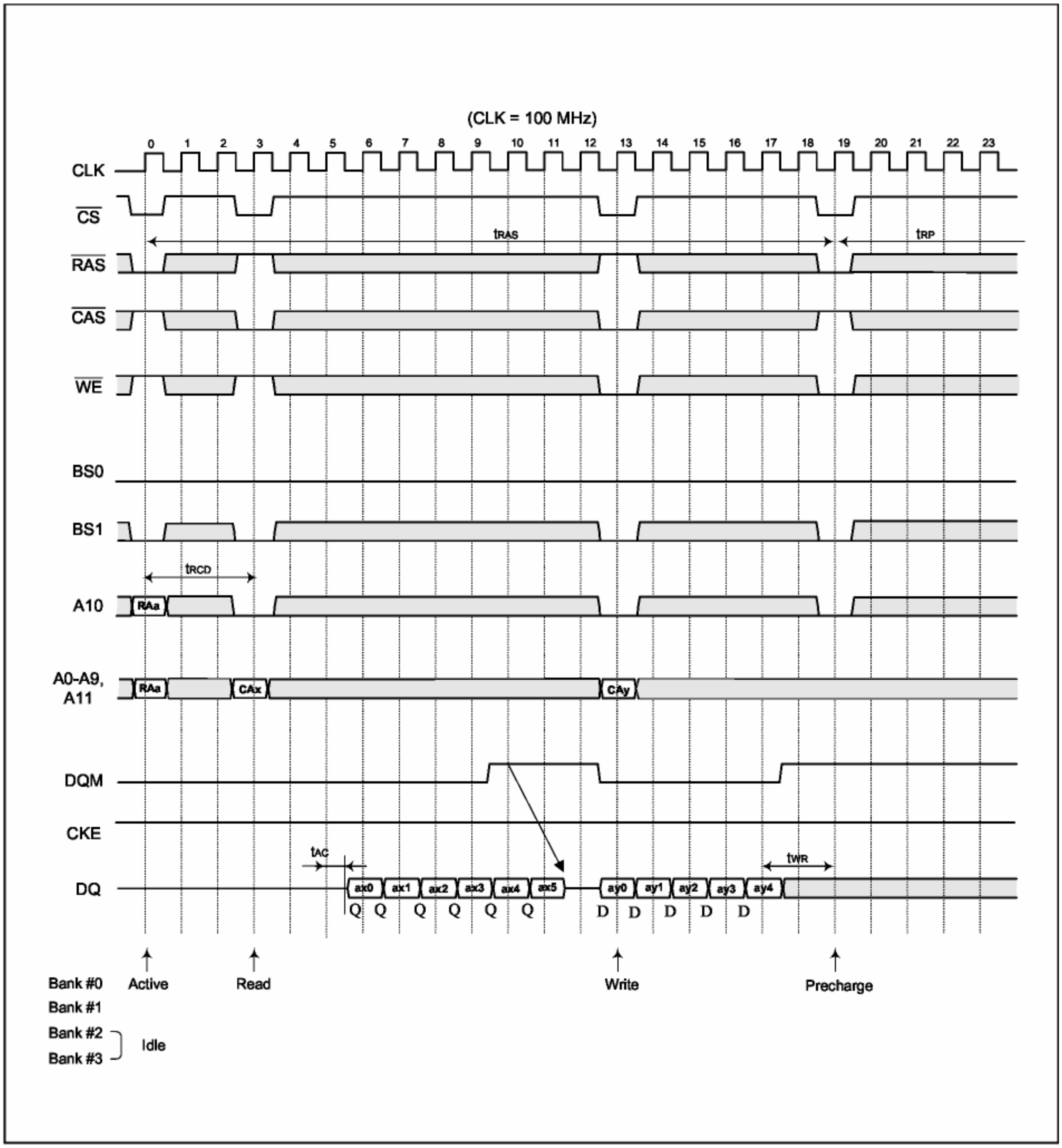
14.11 Page Mode Read

(Burst Length = 4, CAS Latency = 3)



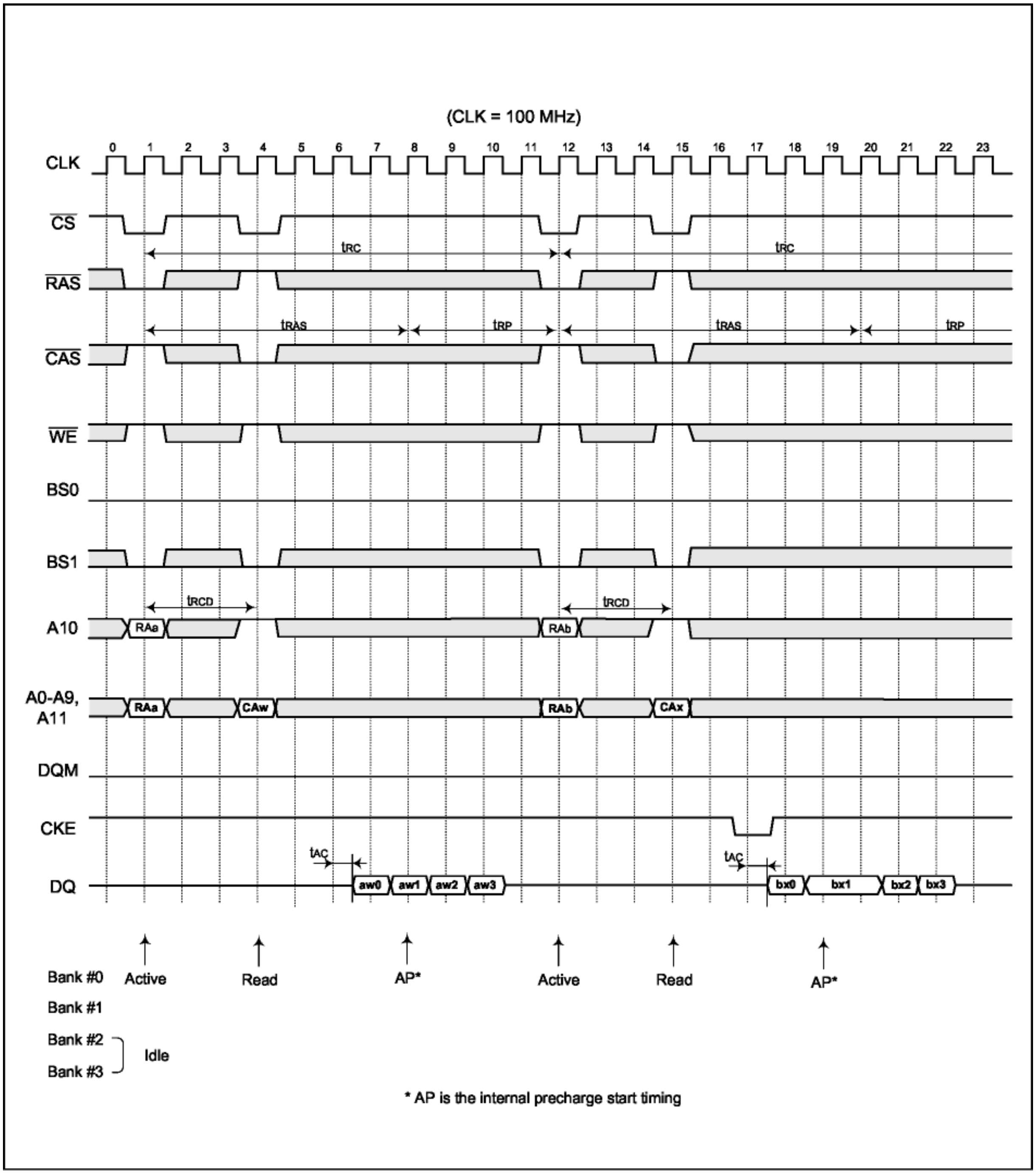
14.12 Page Mode Read/Write

(Burst Length = 8, CAS Latency = 3)



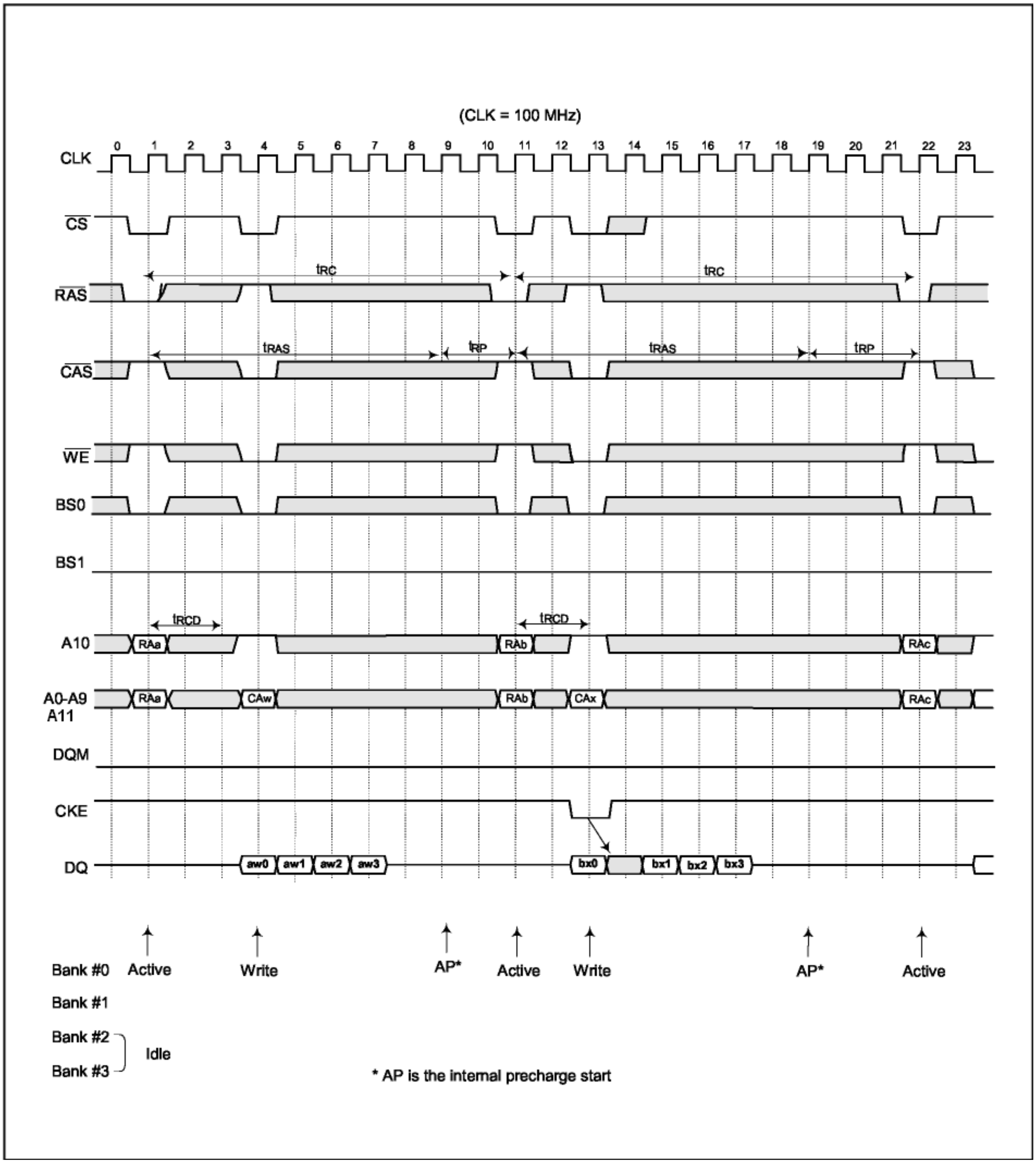
14.13 AutoPrecharge Read

(Burst Length = 4, CAS Latency = 3)

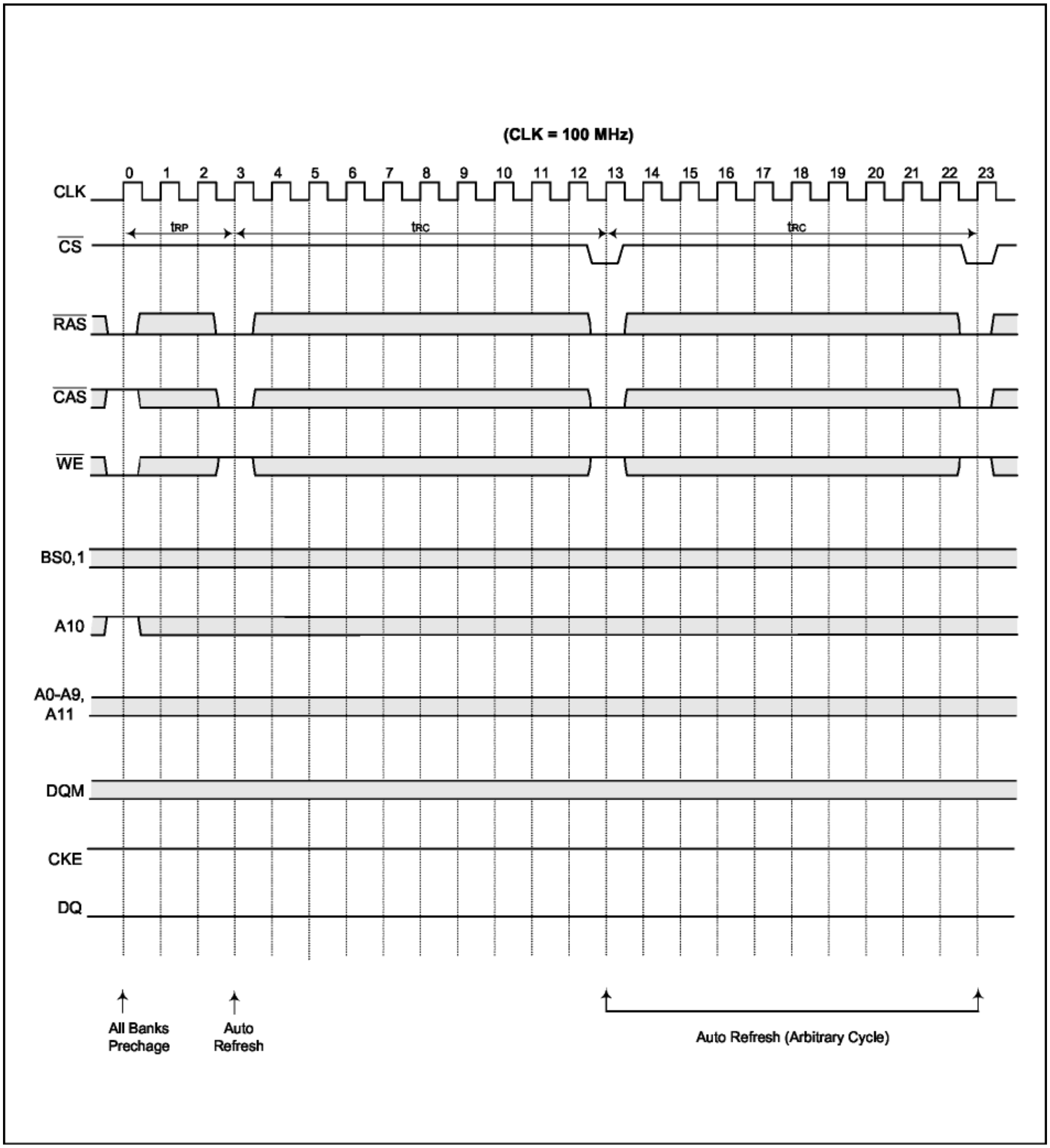


14.14 AutoPrecharge Write

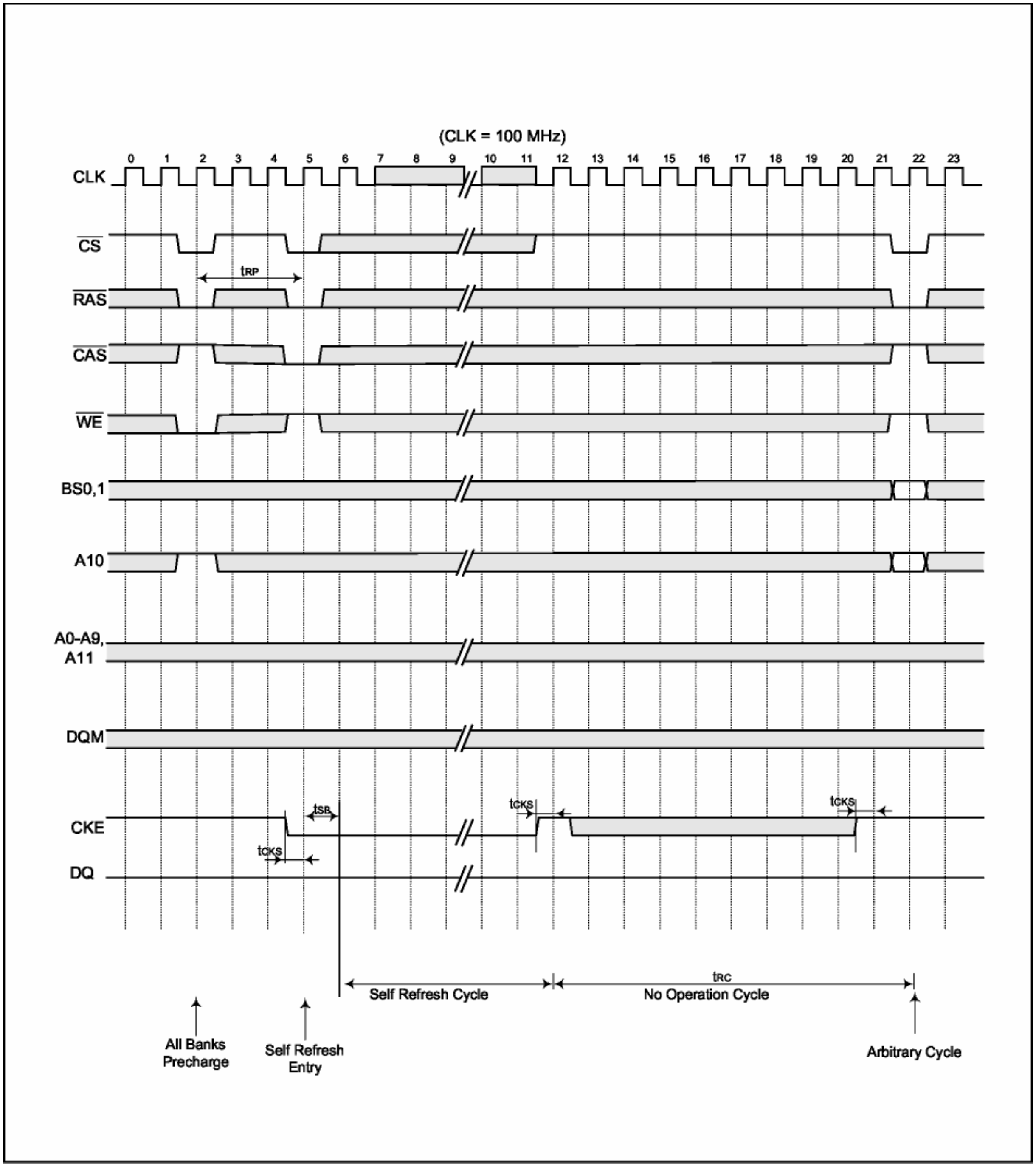
(Burst Length = 4)



14.15 AutoRefresh Cycle

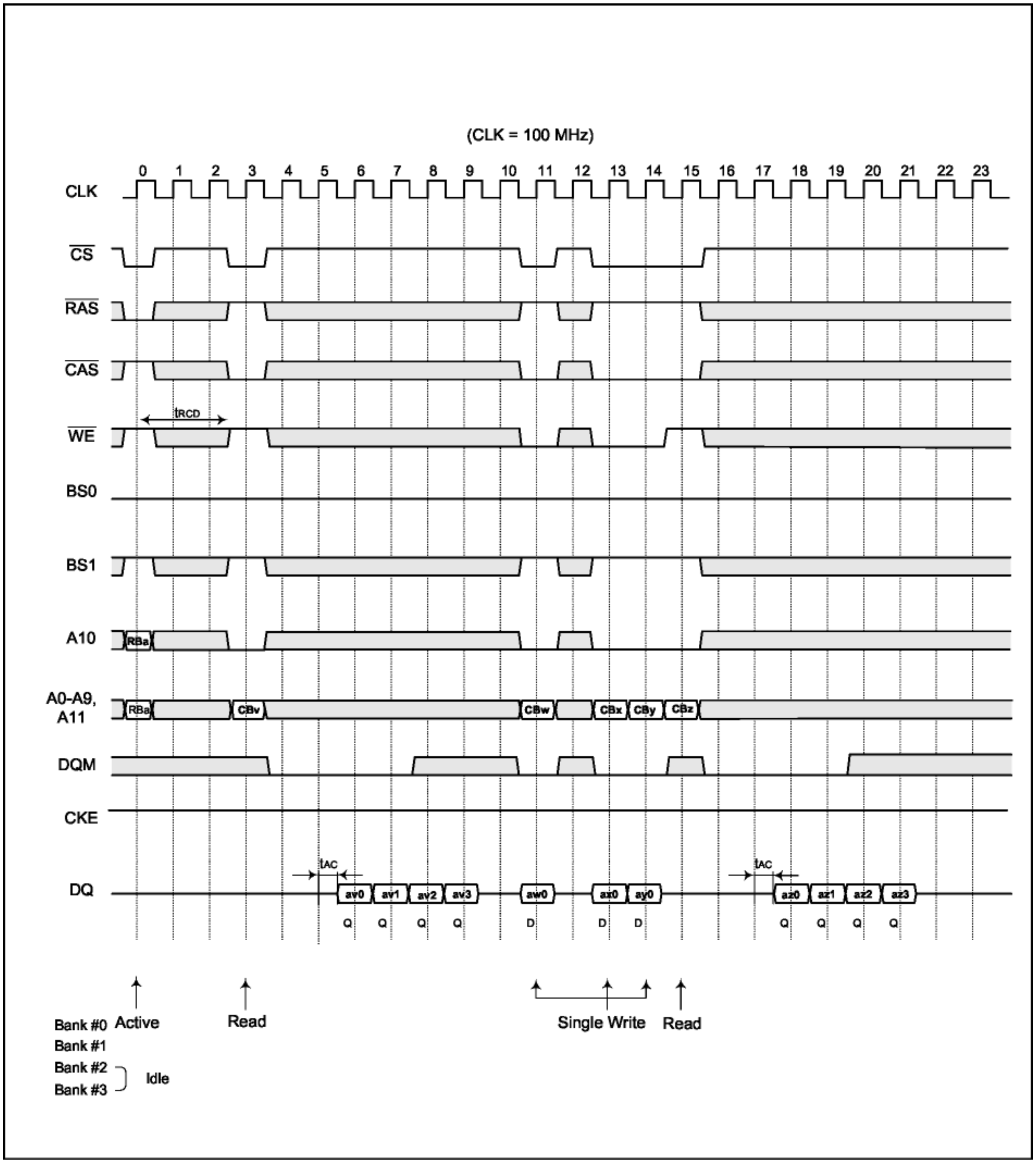


14.16 SelfRefresh Cycle

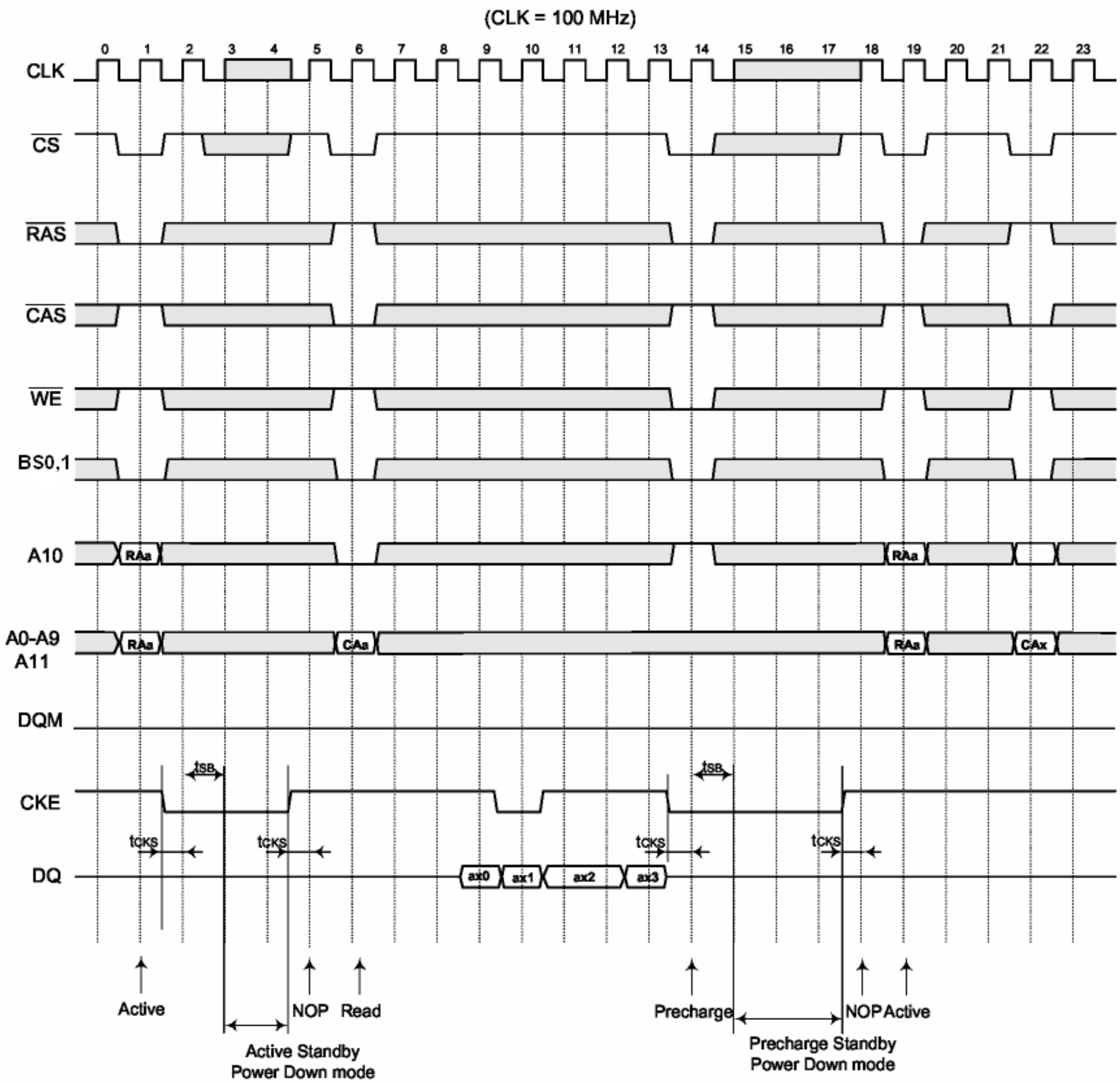


14.17 Bust Read and Single Write

(Burst Length = 4, CAS Latency = 3)



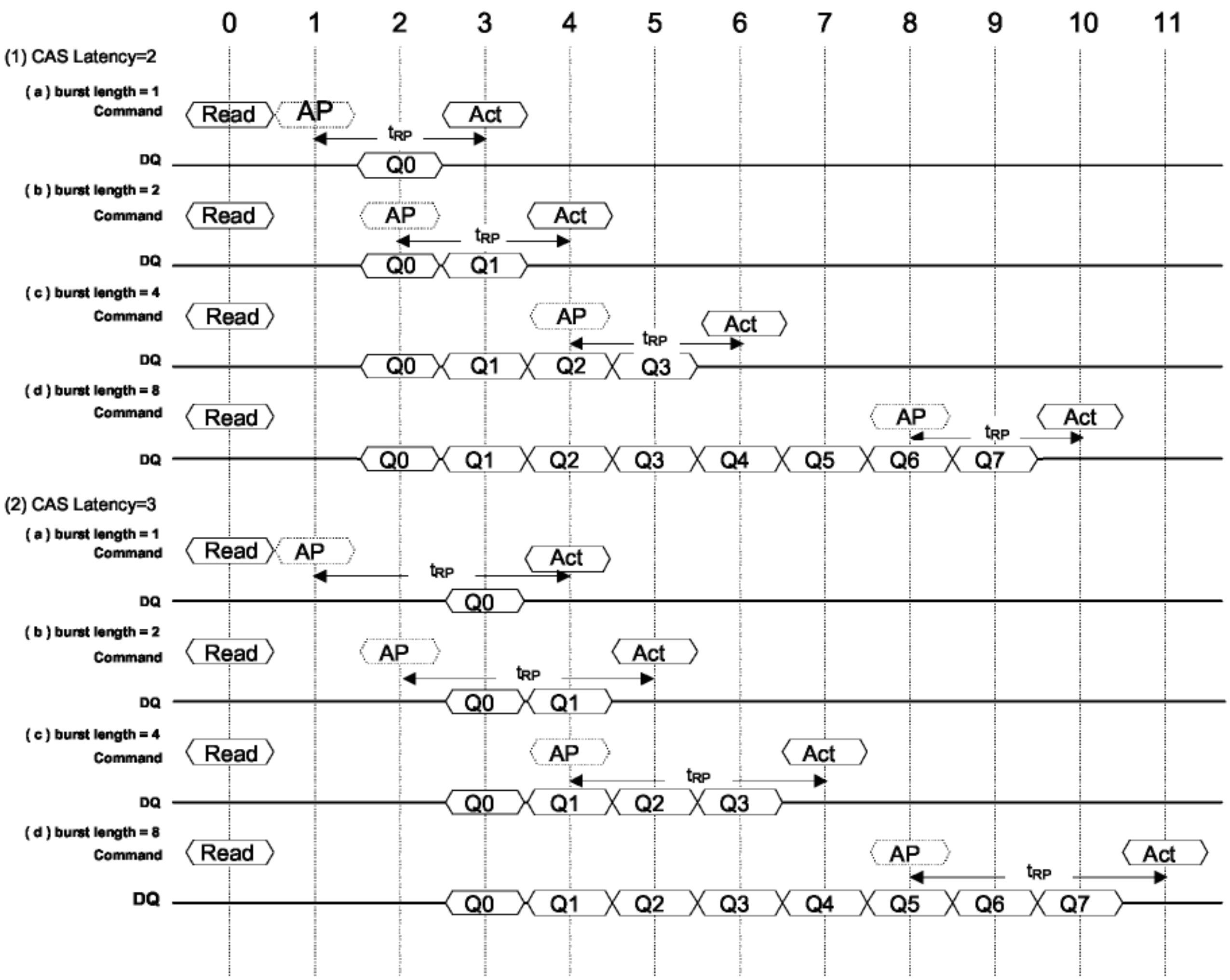
14.18PowerDown Mode



Note: The PowerDown Mode is entered by asserting CKE "low".
All Input/Output buffers (except CKE buffers) are turned off in the PowerDown mode.
When CKE goes high, command input must be No operation at next CLK rising edge.

14.19 Autoprecharge Timing

(Read Cycle)



Note:

Read — represents the Read with Auto precharge command.

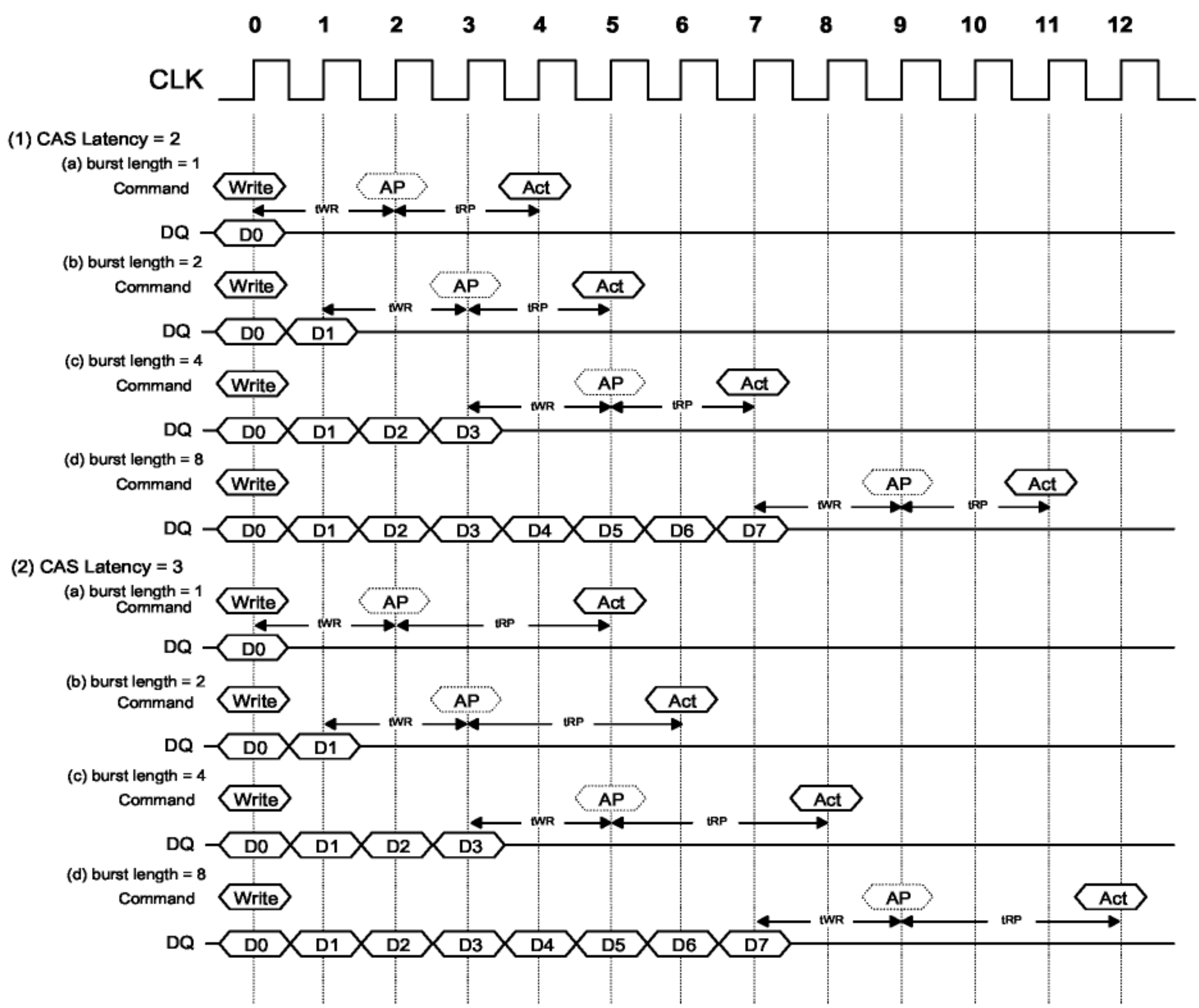
AP — represents the start of internal precharging.

Act — represents the Bank Activate command.

When the Auto precharge command is asserted, the period from Bank Activate command to the start of internal precgarging must be at least t_{RAS}(min).

14.20 Autoprecharge Timing

(Write Cycle)



Note)

Write represents the Write with Auto precharge command.

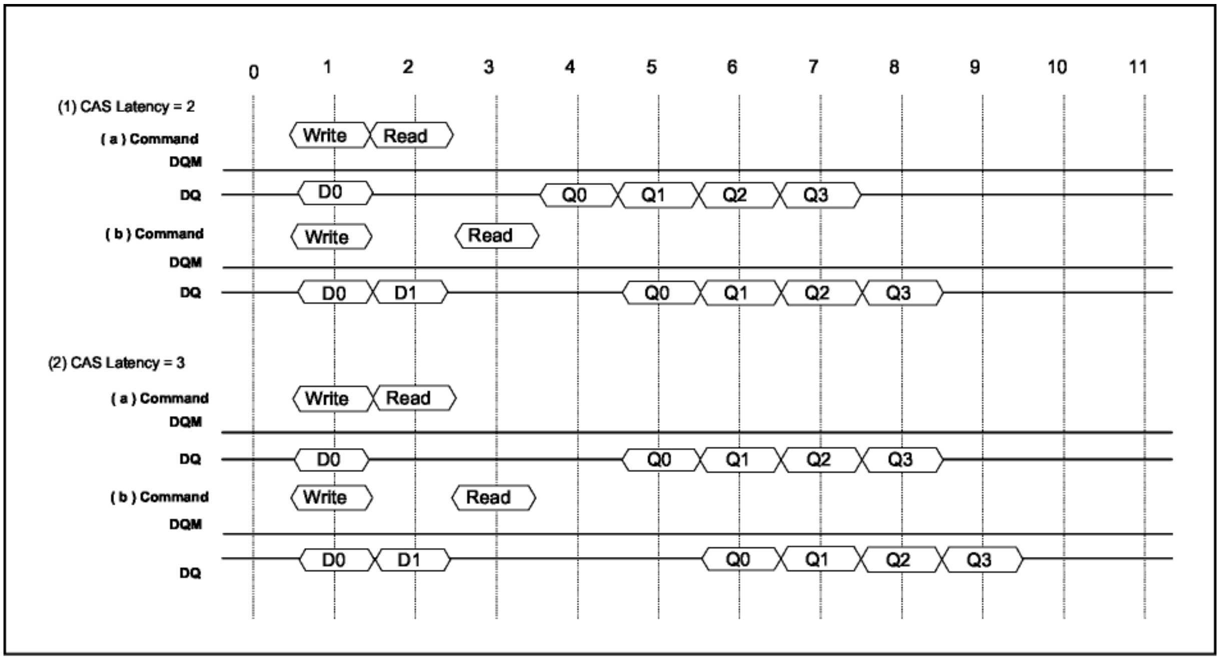
AP represents the start of internal precharing.

Act represents the Bank Active command.

When the /auto precharge command is asserted,the period from Bank Activate command to the start of intermal precgarging must be at least tRAS (min).

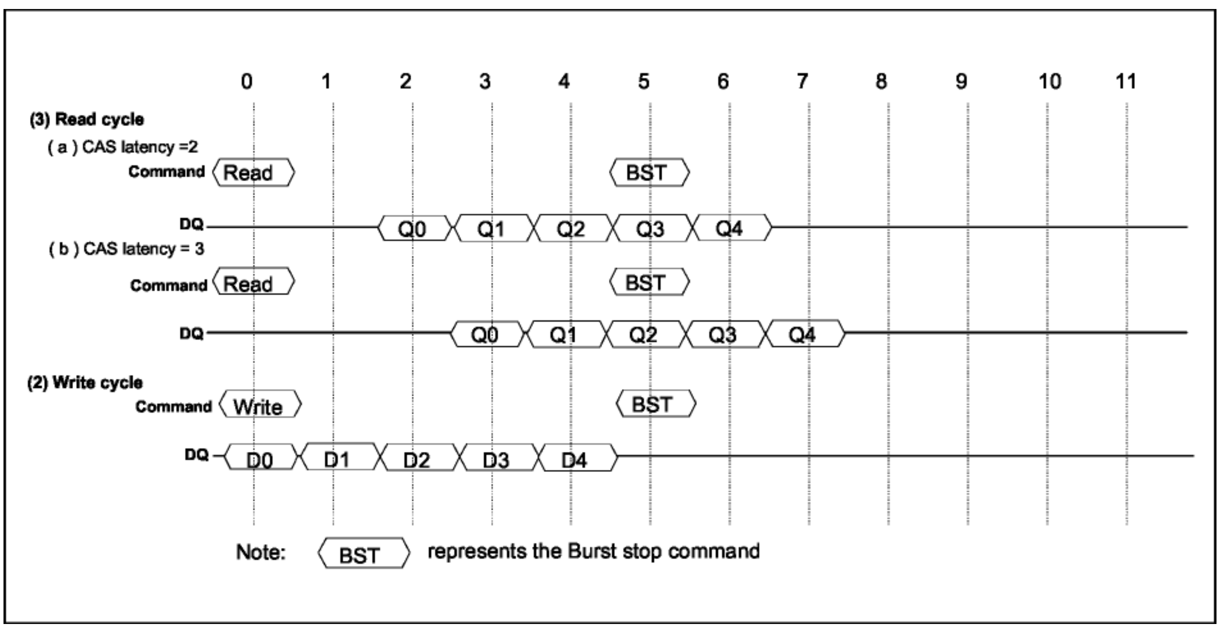
14.21 Timing Chart of Write-to-Read Cycle

In the case of Burst Length = 4



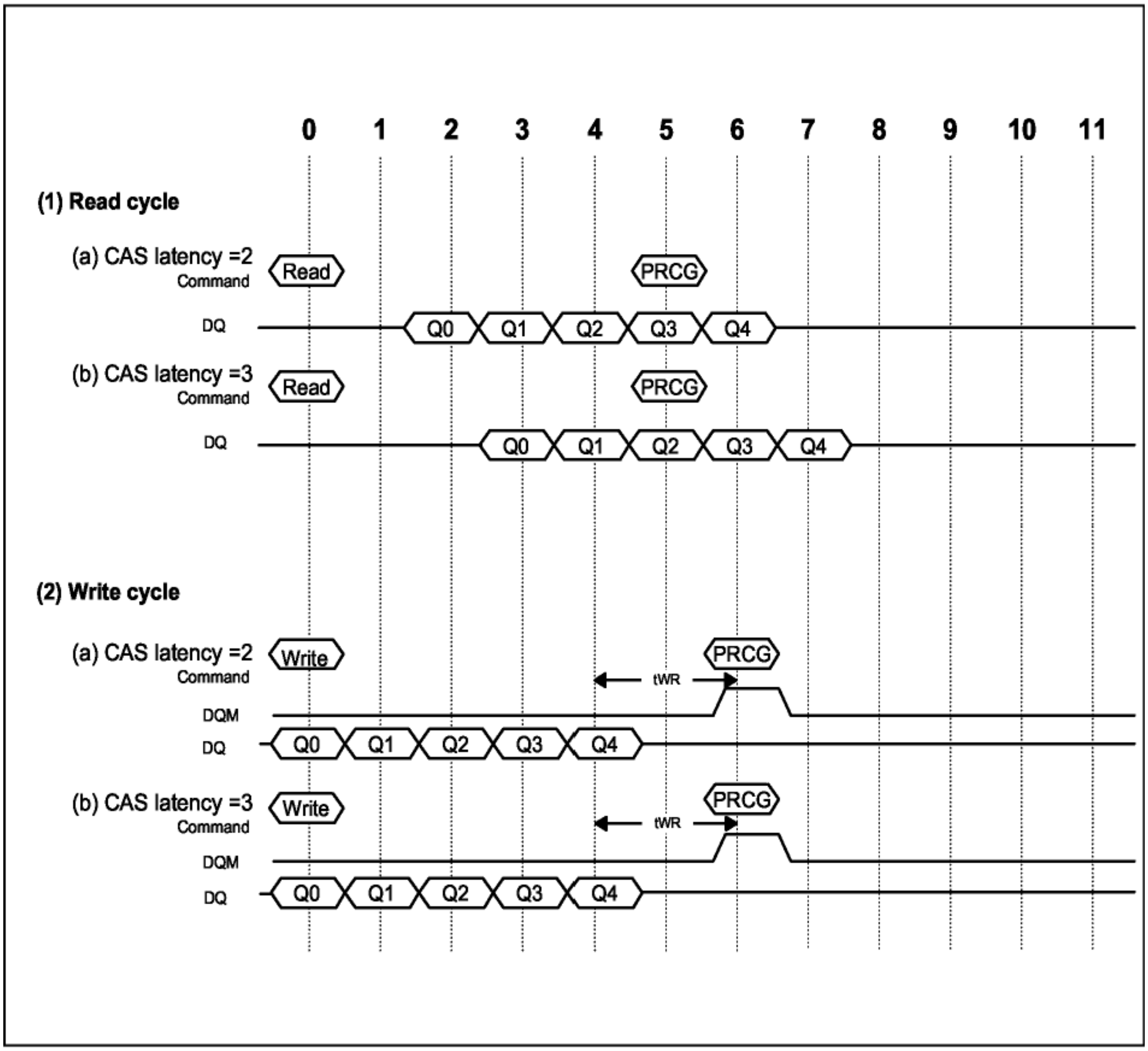
14.22 Timing Chart of Burst Stop Cycle

(Burst Stop Command)



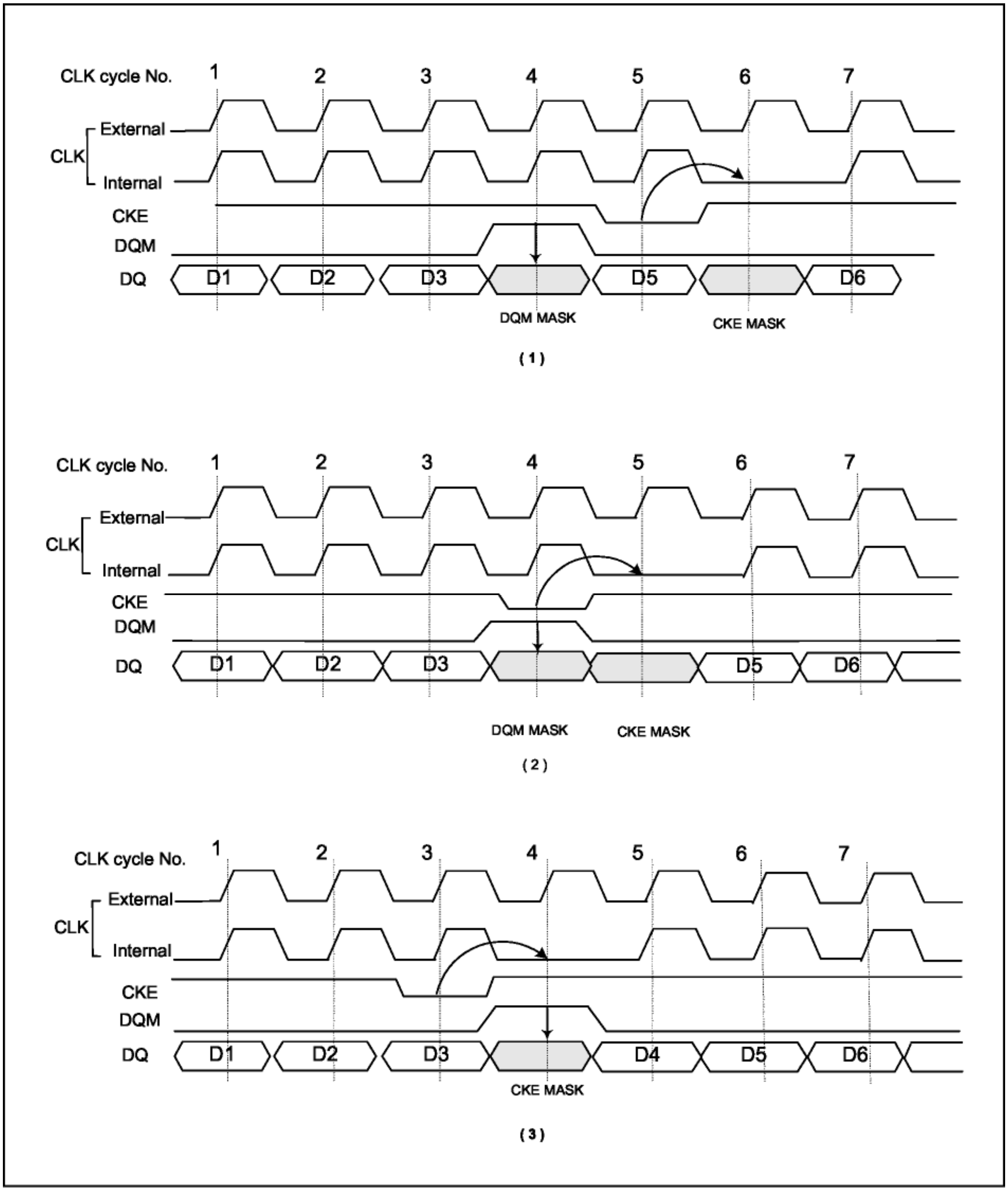
14.23 Timing Chart of Burst Stop Cycle

(Precharge Command)



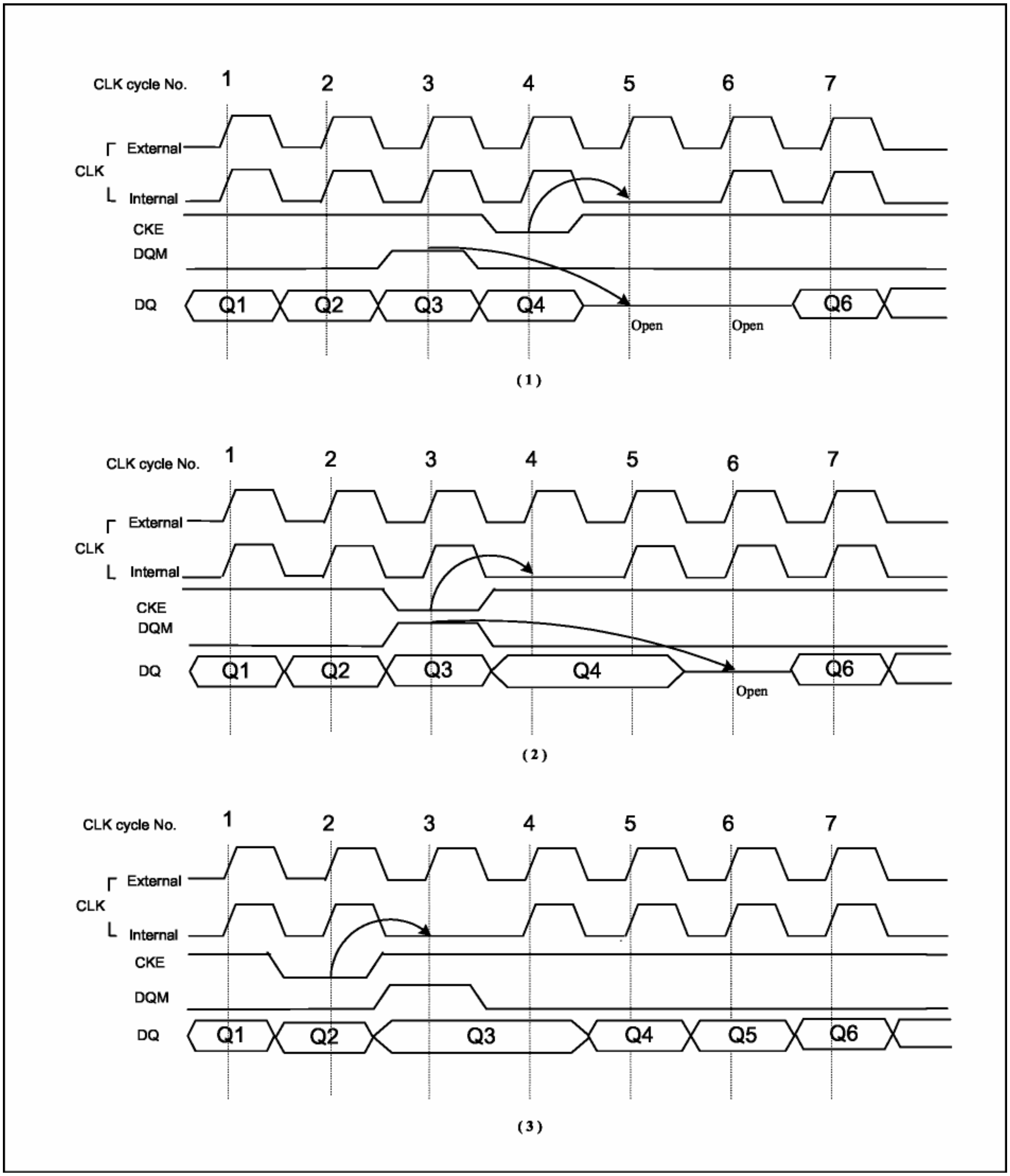
14.24 CKE/DQM Input Timing

(Write Cycle)

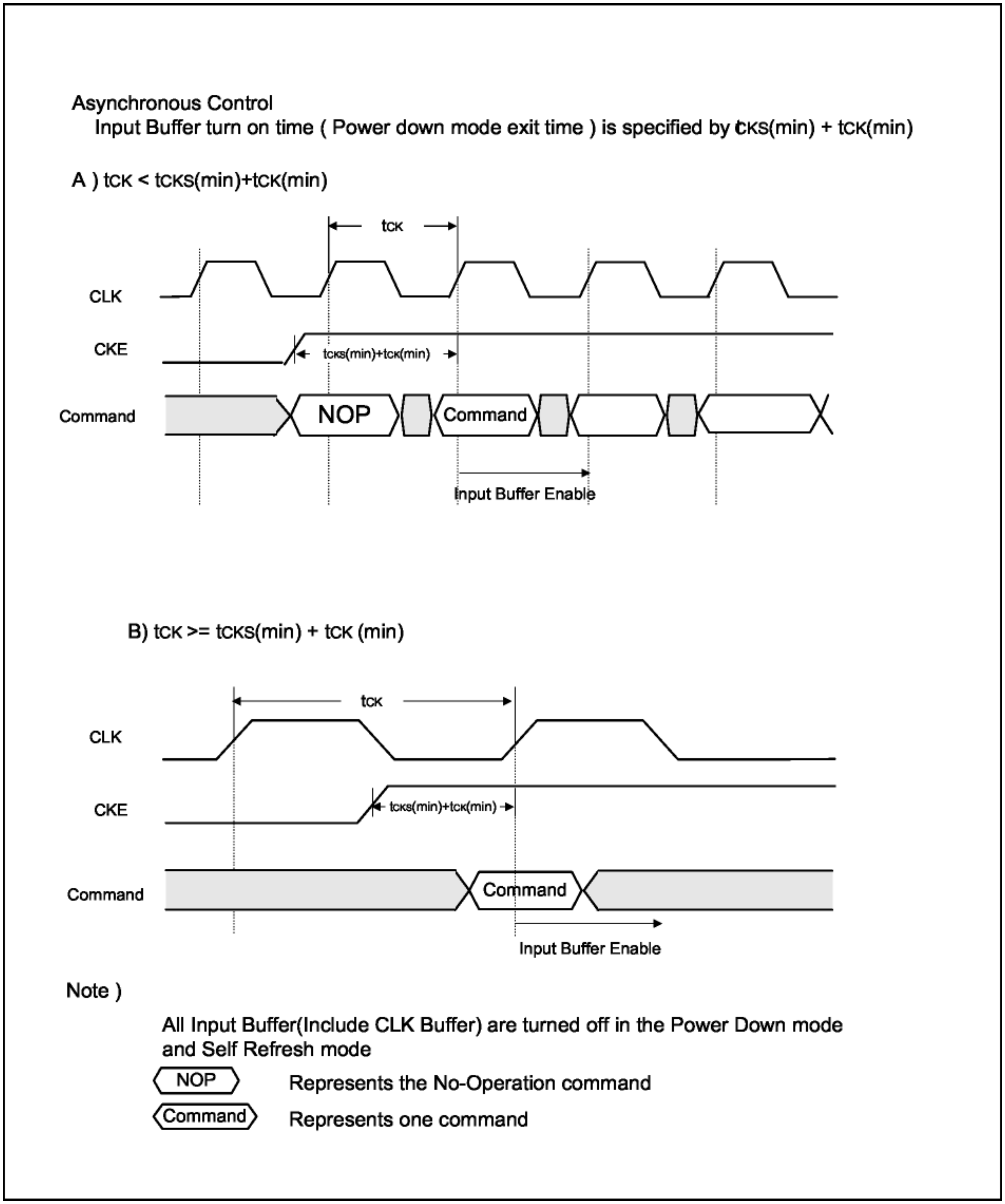


14.25CKE/DQM Input Timing

(Read Cycle)

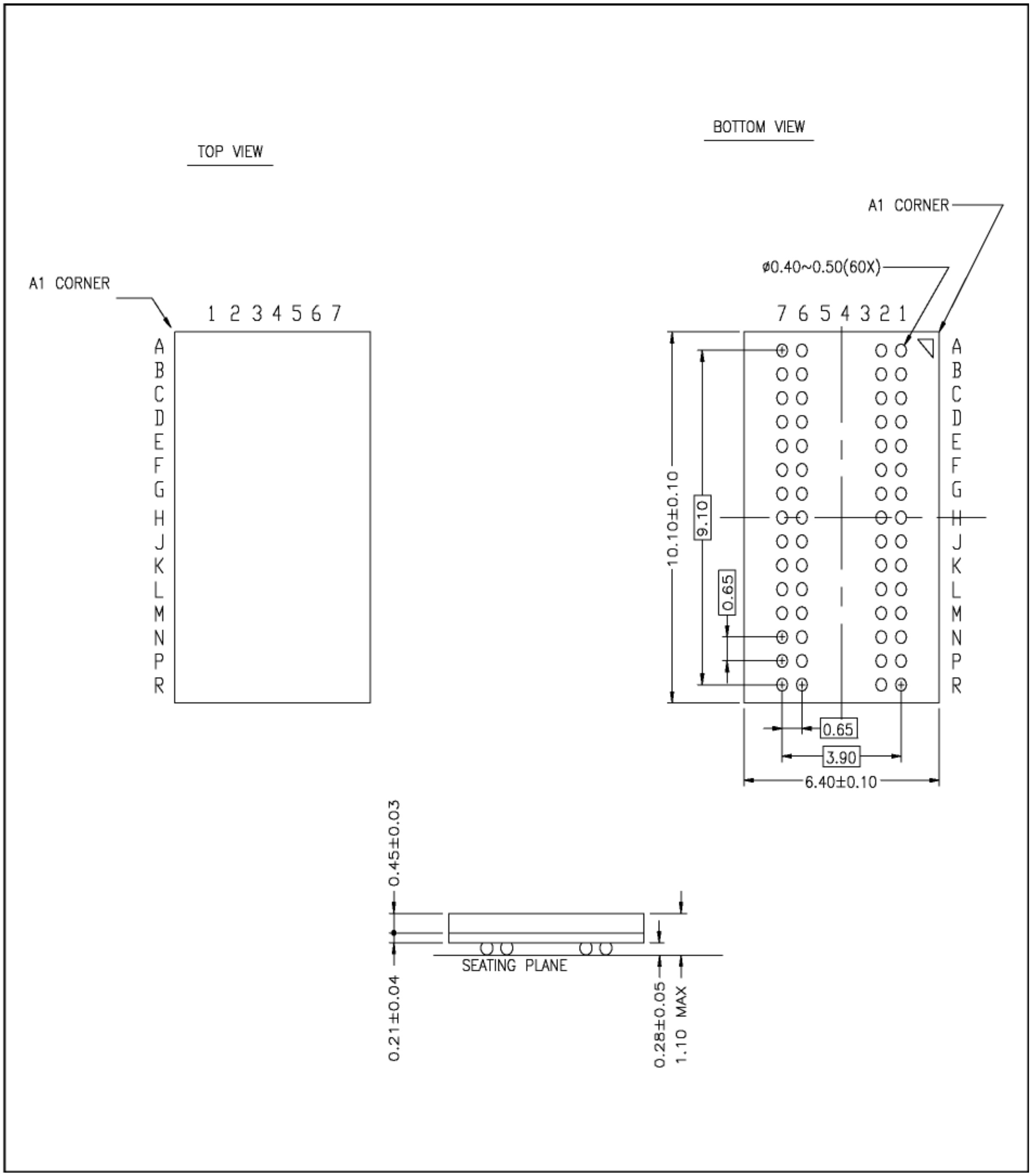


14.26 Self Refresh/Power Down Mode Exit Timing



15. PACKAGE DIMENSIONS

15.1 VFBGA 60 balls pitch=0.65mm



16. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A00	05/05/2005	—	Preliminary datasheet
A01	06/14/2006	—	Modified all parameter
A02	01/10/2008	—	Add -6 parameter

Important Notice

Pointec products are not designed, intended, authorized or warranted for use as components in systems or equipment intended for surgical implantation, atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, or for other applications intended to support or sustain life. Further more, Pointec products are not intended for applications wherein failure of Pointec products could result or lead to a situation wherein personal injury, death or severe property or environmental damage could occur.

Pointec customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Pointec for any damages resulting from such improper use or sales.