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1. GENERAL DESCRIPTION

The PT476416BG is a 1G bits DDR2 SDRAM, organized as 8,388,608 words × 8 banks × 16 bits. This device achieves high speed transfer rates up to 1066Mb/sec/pin (DDR2-1066) for general applications. PT476416BG is sorted into the following speed grades: -18, -25 and -3. The -18 is compliant to the DDR2-1066/CL7 specification, the -25 is compliant to the DDR2-800/CL6 specification, the -3 is compliant to the DDR2-667/CL5 specification.

All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks (CLK rising and /CLK falling). All I/Os are synchronized with a single ended DQS or differential DQS- /DQS pair in a source synchronous fashion.

2. FEATURES

- Power Supply: V_{DD}, V_{DDQ} = 1.8 V ± 0.1 V
- Double Data Rate architecture: two data transfers per clock cycle
- CAS Latency: 3, 4, 5, 6 and 7
- Burst Length: 4 and 8
- Bi-directional, differential data strobes (DQS and /DQS) are transmitted / received with data
- Edge-aligned with Read data and center-aligned with Write data
- DLL aligns DQ and DQS transitions with clock
- Differential clock inputs (CLK and /CLK)
- Data masks (DM) for write data.
- Commands entered on each positive CLK edge, data and data mask are referenced to both edges of DQS
- Posted /CAS programmable additive latency supported to make command and data bus efficiency
- Read Latency = Additive Latency plus CAS Latency (RL = AL + CL)
- Off-Chip-Driver impedance adjustment (OCD) and On-Die-Termination (ODT) for better signal quality
- Auto-precharge operation for read and write bursts
- Auto Refresh and Self Refresh modes
- Precharged Power Down and Active Power Down
- Write Data Mask
- Write Latency = Read Latency - 1 (WL = RL - 1)
- Interface: SSTL_18
- Packaged in WBGA 84 Ball (8X12.5 mm^2), using Lead free materials with RoHS compliant

3. KEY PARAMETERS

SYM	SPEED GRADE			DDR2-1066	DDR2-800	DDR2-667
	Bin(CL-tRCD-tRP)			7-7-7	6-6-6	5-5-5
	PARAMETER			-18	-25	-3
tCK	Clock Cycle Time	CL = 7	Min	1.875 nS	2. 5 nS	-
			Max	7.5 nS	8 nS	-
		CL = 6	Min	1.875 nS	2. 5 nS	-
			Max	7.5 nS	8 nS	-
		CL = 5	Min	3 nS	3 nS	3 nS
			Max	7.5 nS	8 nS	8 nS
		CL = 4	Min	3.75 nS	3.75 nS	3.75 nS
			Max	7.5 nS	8 nS	8 nS
		CL = 3	Min	-	5 nS	5 nS
			Max	-	8 nS	8 nS
tRCD	Active to Read/Write Command Delay Time		Min	13.125 nS	15 nS	15 nS
tRP	Precharge to Active Command Period		Min	13.125 nS	15 nS	15 nS
tRC	Active to Ref/Active Command Period		Min	53.125 nS	55 nS	55 nS
tRAS	Active to Precharge Command Period		Min	40 nS	40 nS	40 nS
IDD0	Operating current		Max	96 mA	82 mA	78 mA
IDD1	Operation current (Single bank)		Max	98 mA	87 mA	83 mA
IDD2Q	Precharge quiet standby current		Max	58 mA	47 mA	43 mA
IDD4R	Operating burst read current		Max	171 mA	142 mA	127 mA
IDD4W	Operating burst write current		Max	187 mA	155 mA	138 mA
IDD5B	Burst refresh current		Max	168 mA	157 mA	151 mA
IDD6	Self refresh current		Max	9 mA	9 mA	9 mA

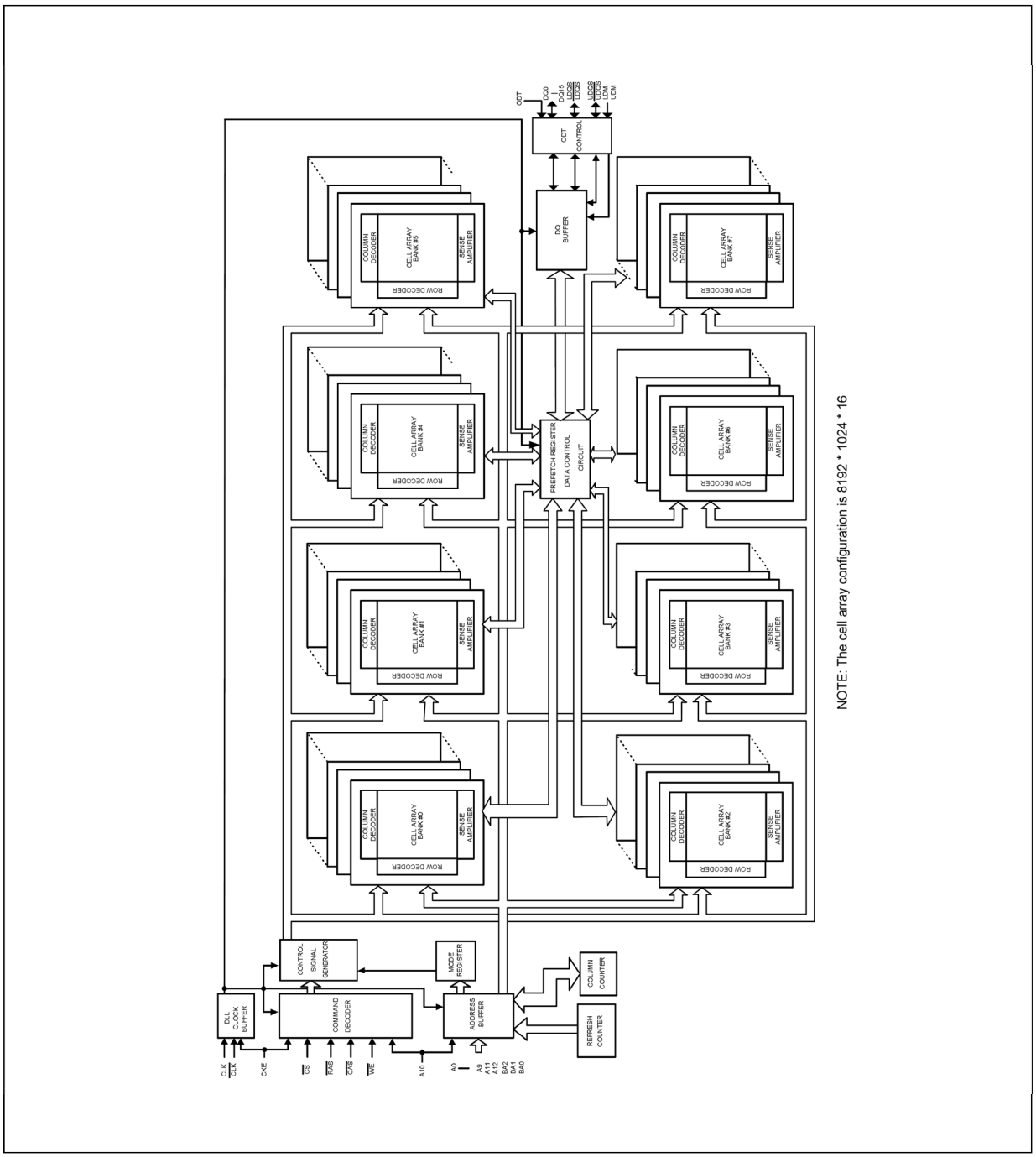
4. Ball Configuration

1	2	3	4	5	6	7	8	9
VDD	NC	VSS		A		VSSQ	/UDQS	VDDQ
DQ14	VSSQ	UDM		B		UDQS	VSSQ	DQ15
VDDQ	DQ9	VDDQ		C		VDDQ	DQ8	VDDQ
DQ12	VSSQ	DQ11		D		DQ10	VSSQ	DQ13
VDD	NC	VSS		E		VSSQ	/LDQS	VDDQ
DQ6	VSSQ	LDM		F		LDQS	VSSQ	DQ7
VDDQ	DQ1	VDDQ		G		VDDQ	DQ0	VDDQ
DQ4	VSSQ	DQ3		H		DQ2	VSSQ	DQ5
VDDL	VREF	VSS		J		VSSDL	CLK	VDD
	CKE	/WE		K		/RAS	/CLK	ODT
BA2	BA0	BA1		L		/CAS	/CS	
	A10/AP	A1		M		A2	A0	VDD
VSS	A3	A5		N		A6	A4	
	A7	A9		P		A11	A8	VSS
VDD	A12	NC		R		NC	NC	

5. BALL DESCRIPTION

BALL NUMBER	SYMBOL	FUNCTION	DESCRIPTION
M8,M3,M7,N2,N8,N3 ,N7,P2,P8,P3,M2,P7, R2	A0−A12	Address	Provide the row address for active commands, and the column address and Auto-precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. Row address: A0−A12. Column address: A0−A9. (A10 is used for Auto-precharge)
L2,L3,L1	BA0−BA2	Bank Select	BA0−BA2 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied.
G8,G2,H7,H3,H1,H9, F1,F9,C8,C2,D7,D3, D1,D9,B1,B9	DQ0−DQ15	Data Input / Output	Bi-directional data bus.
K9	ODT	On Die Termination Control	ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM.
F7,E8	LDQS, /LDQS	LOW Data Strobe	Data Strobe for Lower Byte: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. LDQS corresponds to the data on DQ0−DQ7. /LDQS is only used when differential data strobe mode is enabled via the control bit at EMR (1)[A10 EMRS command].
B7,A8	UDQS, /UDQS	UP Data Strobe	Data Strobe for Upper Byte: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. UDQS corresponds to the data on DQ8−DQ15./UDQS is only used when differential data strobe mode is enabled via the control bit at EMR (1)[A10 EMRS command].
L8	/CS	Chip Select	All commands are masked when /CS is registered HIGH. /CS provides for external bank selection on systems with multiple ranks. /CS is considered part of the command code.
K7,L7,K3	/RAS, /CAS, /WE	Command Inputs	/RAS, /CAS and /WE (along with /CS) define the command being entered.
B3,F3	UDM, LDM	Input Data Mask	DM is an input mask signal for write data. Input data is masked when DM is sampled high coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
J8,K8	CLK, /CLK	Differential Clock Inputs	CLK and /CLK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of /CLK and negative edge of CLK . Output (read) data is referenced to the crossings of CLK and /CLK (both directions of crossing).
K2	CKE	Clock Enable	CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM.
J2	VREF	Reference Voltage	VREF is reference voltage for inputs.
A1,E1,J9,M9,R1	VDD	Power Supply	Power Supply: 1.8V ± 0.1V.
A3,E3,J3,N1,P9	VSS	Ground	Ground.
A9,C1,C3,C7,C9,E9, G1,G3,G7,G9	VDDQ	DQ Power Supply	DQ Power Supply: 1.8V ± 0.1V.
A7,B2,B8,D2,D8,E7, F2,F8,H2,H8	VSSQ	DQ Ground	DQ Ground. Isolated on the device for improved noise immunity.
A2,E2,L1,R3,R7,R8	NC	No Connection	No connection
J7	VSSDL	DLL Ground	DLL Ground.
J1	VDDL	DLL Power Supply	DLL Power Supply: 1.8V ± 0.1V.

6. BLOCK DIAGRAM



7. FUNCTIONAL DESCRIPTION

7.1. Power-up and Initialization Sequence

DDR2 SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. The following sequence is required for Power-up and Initialization.

1. Apply power and attempt to maintain CKE below 0.2 × VDDQ and ODT[*1] at a LOW state (all other inputs may be undefined.) Either one of the following sequence is required for Power-up.

   A. The VDD voltage ramp time must be no greater than 200 mS from when VDD ramps from 300 mV to VDD min; and during the VDD voltage ramp, |VDD -VDDQ| ≦ 0.3 volts.

   - VDD, VDDL and VDDQ are driven from a single power converter output
   - VTT is limited to 0.95V max
   - VREF*2 tracks VDDQ/2
   - VDDQ ≧ VREF must be met at all times

   B. Voltage levels at I/Os and outputs must be less than VDDQ during voltage ramp time to avoid DRAM latch-up. During the ramping of the supply voltages, VDD ≧ VDDL ≧ VDDQ must be maintained and is applicable to both AC and DC levels until the ramping of the supply voltages is complete.

   - Apply VDD/VDDL[*3] before or at the same time as VDDQ
   - Apply VDDQ[*4] before or at the same time as VTT
   - VREF[*2] tracks VDDQ/2
   - VDDQ ≧ VREF must be met at all times.

2. Start Clock and maintain stable condition for 200 μS (min.).
3. After stable power and clock (CLK,CLK), apply NOP or Deselect and take CKE HIGH.
4. Wait minimum of 400 nS then issue precharge all command. NOP or Deselect applied during 400 nS period.
5. Issue an EMRS command to EMR (2). (To issue EMRS command to EMR (2), provide LOW to BA0, HIGH to BA1, LOW to BA2.)
6. Issue an EMRS command to EMR (3). (To issue EMRS command to EMR (3), provide HIGH to BA0 and BA1, LOW to BA2.)
7. Issue EMRS to enable DLL. (To issue DLL Enable command, provide LOW to A0, HIGH to BA0 and LOW to BA1, LOW to BA2. And A9=A8=A7=LOW must be used when issuing this command.)
8. Issue a Mode Register Set command for DLL reset. (To issue DLL Reset command, provide HIGH to A8 and LOW to BA0 and BA1 and BA2.)
9. Issue a precharge all command.
10. Issue 2 or more Auto Refresh commands.
11. Issue a MRS command with LOW to A8 to initialize device operation. (i.e. to program operating parameters without resetting the DLL.)
12. At least 200 clocks after step 8, execute OCD Calibration (Off Chip Driver impedance adjustment). If OCD calibration is not used, EMRS to EMR (1) to set OCD Calibration Default (A9=A8=A7=HIGH) followed by EMRS to EMR (1) to exit OCD Calibration Mode (A9=A8=A7=LOW) must be issued with other operating parameters of EMR(1).
13. The DDR2 SDRAM is now ready for normal operation.

Note:

1. To guarantee ODT off, VREF must be valid and a LOW level must be applied to the ODT pin.
2. VREF must be within ± 300 mV with respect to VDDQ/2 during supply ramp time.
3. VDD/VDDL voltage ramp time must be no greater than 200 mS from when VDD ramps from 300 mV to VDD min.
4. The VDDQ voltage ramp time from when VDD min is achieved on VDD to when VDDQ min is achieved on VDDQ must be no greater than 500 mS.

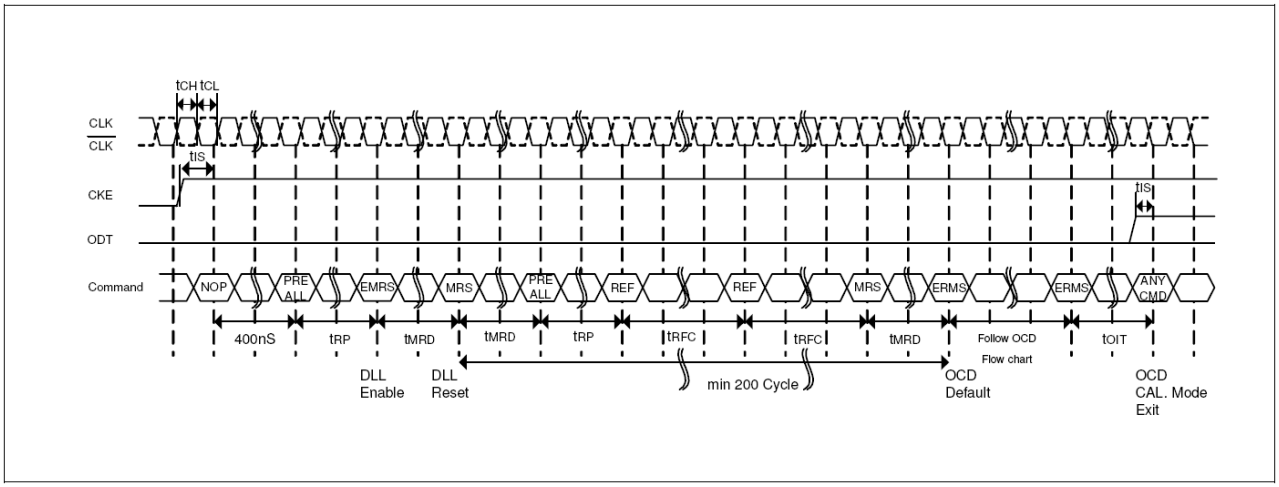


Figure 1 - Initialization sequence after power-up

7.2. Mode Register and Extended Mode Registers Operation

For application flexibility, burst length, burst type, CAS Latency, DLL reset function, write recovery time (WR) are user defined variables and must be programmed with a Mode Register Set (MRS) command. Additionally, DLL disable function, driver impedance, additive CAS Latency, ODT (On Die Termination), single-ended strobe and OCD (off chip driver impedance adjustment) are also user defined variables and must be programmed with an Extended Mode Register Set (EMRS) command. Contents of the Mode Register (MR) or Extended Mode Registers EMR (1), EMR (2) and EMR (3) can be altered by re-executing the MRS or EMRS Commands. Even if the user chooses to modify only a subset of the MR or EMR (1), EMR (2) and EMR (3) variables, all variables within the addressed register must be redefined when the MRS or EMRS commands are issued.

MRS, EMRS and Reset DLL do not affect array contents, which mean re-initialization including those can be executed at any time after power-up without affecting array contents.

7.2.1. Mode Register Set Command (MRS)

(/CS = "L", /RAS = "L", /CAS = "L", /WE = "L", BA0 = "L", BA1 = "L", BA2 = "L", A0 to A12 = Register Data)

The mode register stores the data for controlling the various operating modes of DDR2 SDRAM. It programs CAS Latency, burst length, burst sequence, test mode, DLL reset, Write Recovery (WR) and various vendor specific options to make DDR2 SDRAM useful for various applications. The default value in the Mode Register after power-up is not defined, therefore the Mode Register must be programmed during initialization for proper operation.

The DDR2 SDRAM should be in all bank precharge state with CKE already HIGH prior to writing into the mode register. The mode register set command cycle time (tMRD) is required to complete the write operation to the mode register. The mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state.

The mode register is divided into various fields depending on functionality. Burst length is defined by A[2:0] with options of 4 and 8 bit burst lengths. The burst length decodes are compatible with DDR SDRAM. Burst address sequence type is defined by A3, CAS Latency is defined by A[6:4]. The DDR2 does not support half clock latency mode. A7 is used for test mode. A8 is used for DLL reset. A7 must be set to LOW for normal MRS operation. Write recovery time WR is defined by A[11:9]. Refer to the table for specific codes.

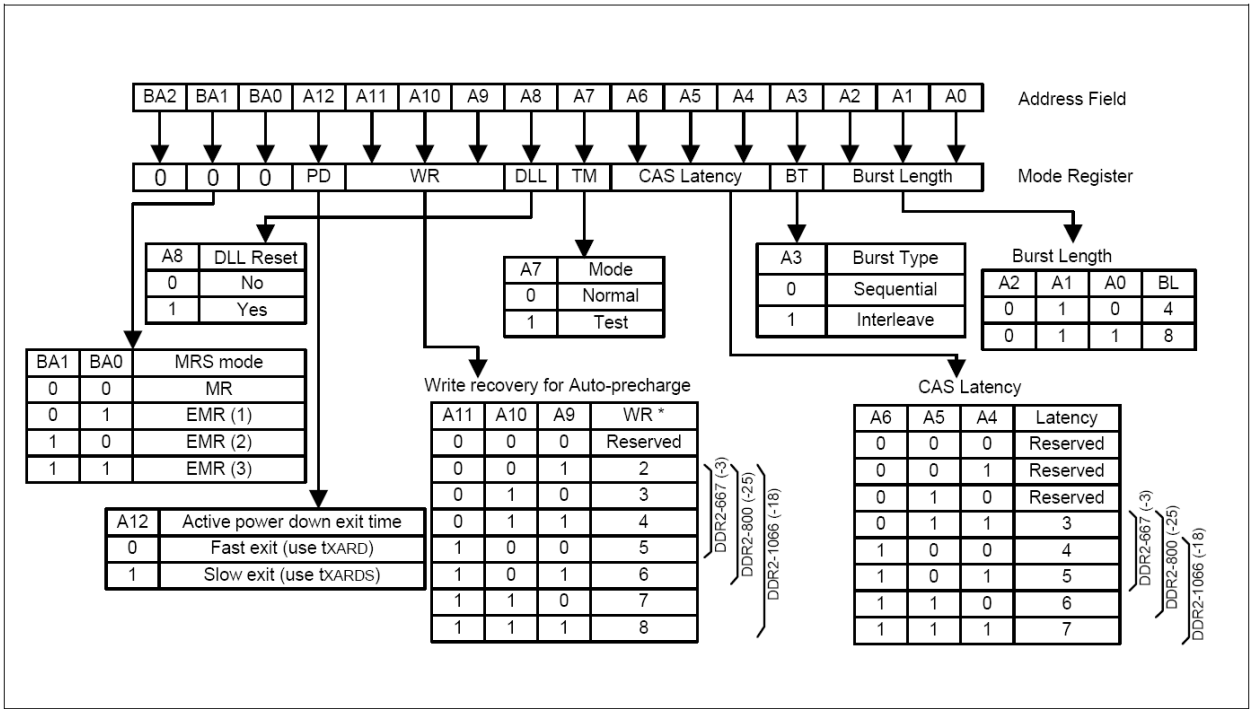


Figure 2 - Mode Register Set (MRS)

Note:

1. WR (write recovery for Auto-precharge) min is determined by tCK max and WR max is determined by tCK min. WR in clock cycles is calculated by dividing tWR (in nS) by tCK (in nS) and rounding up to the next integer (WR[cycles] = RU{ tWR[nS] / tCK [nS] }, where RU stands for round up). The mode register must be programmed to this value. This is also used with tRP to determine tDAL.

7.2.2. Extend Mode Register Set Commands (EMRS)

7.2.2.1. Extend Mode Register Set Command (1), EMR (1)

(/CS = "L", /RAS = "L", /CAS = "L", /WE = "L", BA0 = "H", BA1 = "L, BA2 = "L" A0 to A12 = Register data)

The extended mode register (1) stores the data for enabling or disabling the DLL, output driver strength, additive latency, ODT, /DQS disable, OCD program. The default value of the extended mode register (1) is not defined, therefore the extended mode register (1) must be programmed during initialization for proper operation. The DDR2 SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register (1). The mode register set command cycle time (tMRD) must be satisfied to complete the write operation to the extended mode register (1). Extended mode register (1) contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. A0 is used for DLL enable or disable. A1 is used for enabling a reduced strength output driver. A[5:3] determines the additive latency, A[9:7] are used for OCD control, A10 is used for /DQS disable. A2 and A6 are used for ODT setting.

7.2.2.2. DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power-up initialization, and upon returning to normal operation after having the DLL disabled. The DLL is automatically disabled when entering Self Refresh operation and is automatically re-enabled and reset upon exit of Self Refresh operation. Any time the DLL is enabled (and subsequently reset), 200 clock cycles must occur before a Read command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tAC or tDQSCK parameters.

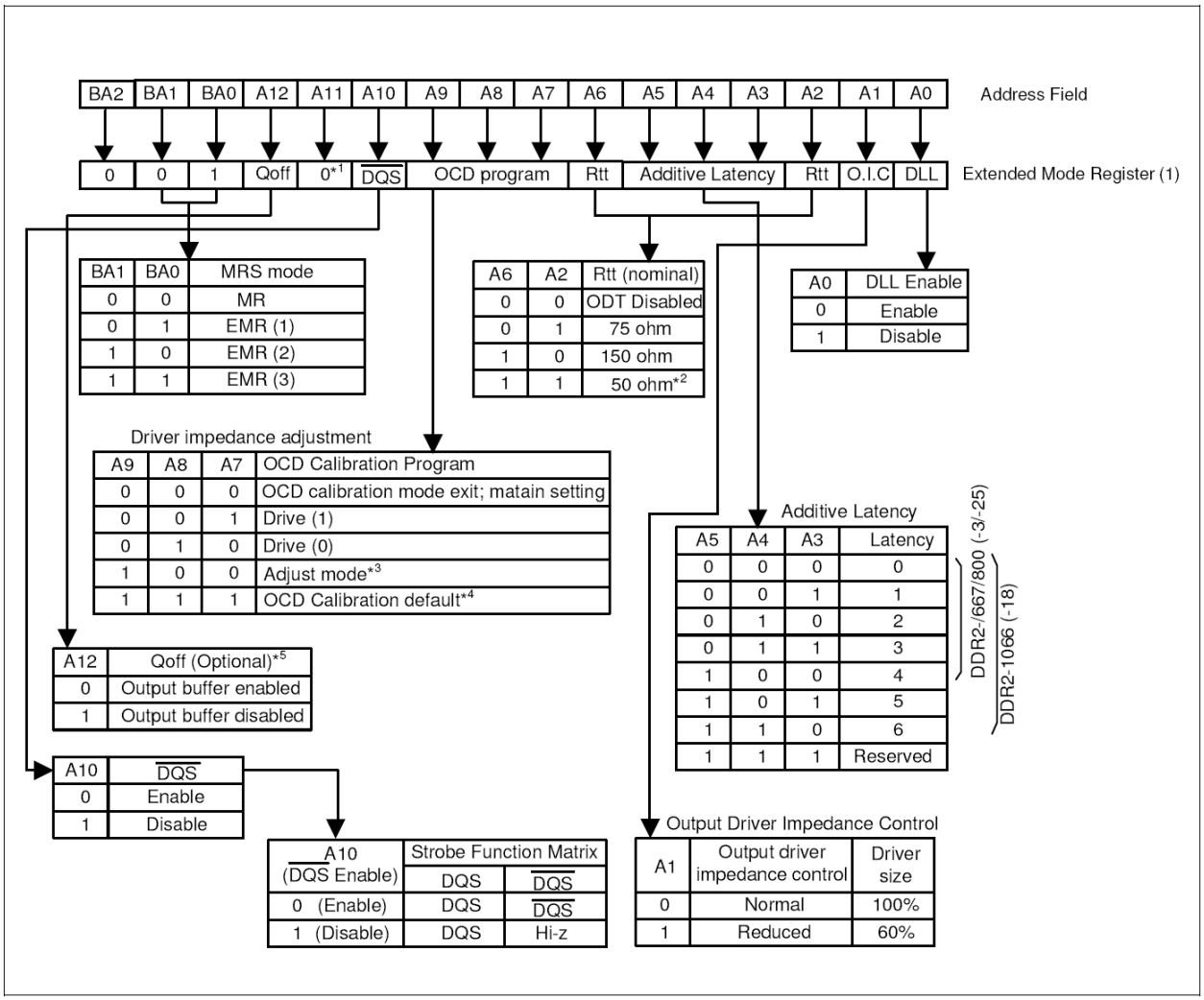


Figure 3 - EMR (1)

Note:

1. A11 default is “0 “ RDQS disabled.
2. Optional for DDR2-667.
3. When Adjust mode is issued, AL from previously set value must be applied.
4. After setting to default, OCD calibration mode needs to be exited by setting A9-A7 to 000. Refer to the section 7.2.3 for detailed information.
5. Output disabled - DQs, LDQS, LDQS , UDQS, UDQS . This feature is used in conjunction with DIMM IDD measurements when IDDQ is not desired to be included.

7.2.2.3. Extend Mode Register Set Command (2), EMR (2)

(/CS = "L", /RAS = "L", /CAS = "L", /WE = "L", BA0 = "L", BA1 = "H", BA2 = "L" A0 to A12 = Register data)

The extended mode register (2) controls refresh related features. The default value of the extended mode register (2) is not defined, therefore the extended mode register (2) must be programmed during initialization for proper operation.

The DDR2 SDRAM should be in all bank precharge state with CKE already high prior to writing into the extended mode register (2). The mode register set command cycle time (tMRD) must be satisfied to complete the write operation to the extended mode register (2). Mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state.

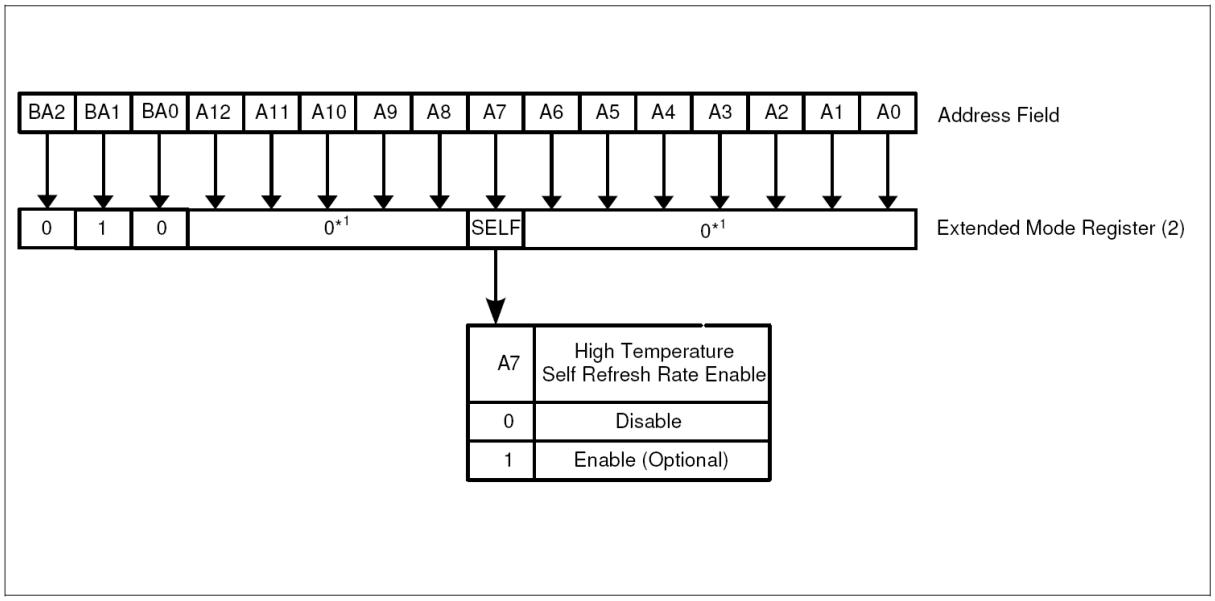


Figure 4 - EMR (2)

Note:

1. The rest bits in EMR (2) is reserved for future use and all bits in EMR (2) except A7, BA0, BA1 and BA2 must be programmed to 0 when setting the extended mode register (2) during initialization. When DRAM is operated at 85 °C 8 TCASE < 95 °C the extended Self Refresh rate must be enabled by setting bit A7 to "1" before the Self Refresh mode can be entered.

7.2.2.4. Extend Mode Register Set Command (3), EMR (3)

(/CS = "L", /RAS = "L", /CAS = "L", /WE = "L", BA0 = "H", BA1 = "H", BA2 = "L", A0 to A12 = Register data)

No function is defined in extended mode register (3). The default value of the EMR (3) is not defined, therefore the EMR (3) must be programmed during initialization for proper operation.

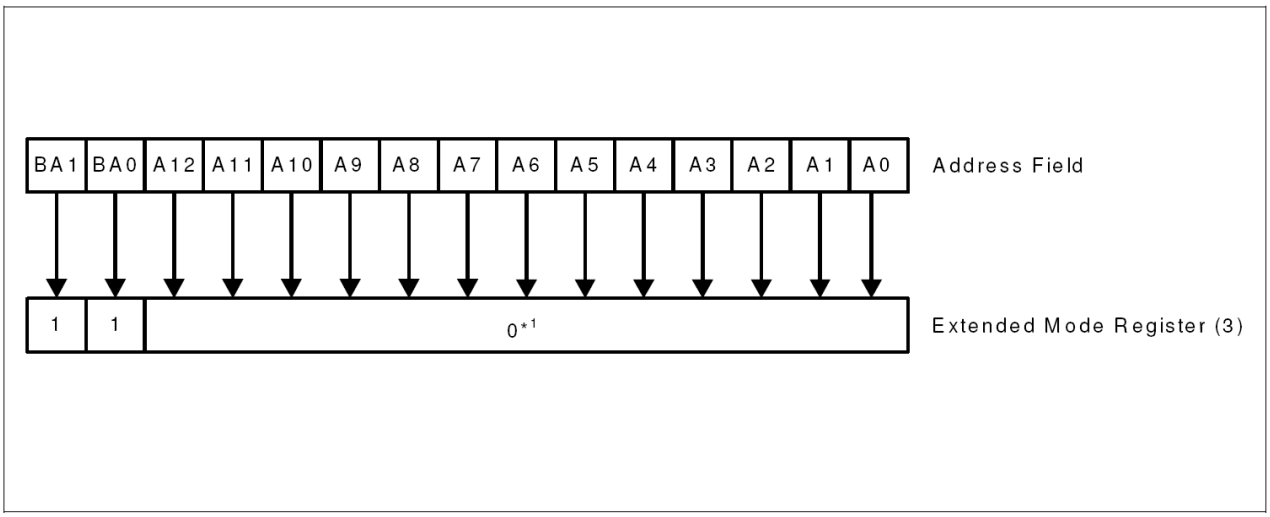


Figure 5 - EMR (3)

Note:

1. All bits in EMR (3) except BA0, BA1 and BA2 are reserved for future use and must be set to 0 when programming the EMR (3).

7.2.3. Off-Chip Driver (OCD) Impedance Adjustment

DDR2 SDRAM supports driver calibration feature and the flow chart in Figure 6 is an example of the sequence. Every calibration mode command should be followed by “OCD calibration mode exit” before any other command being issued. MRS should be set before entering OCD impedance adjustment and On Die Termination (ODT) should be carefully controlled depending on system environment.

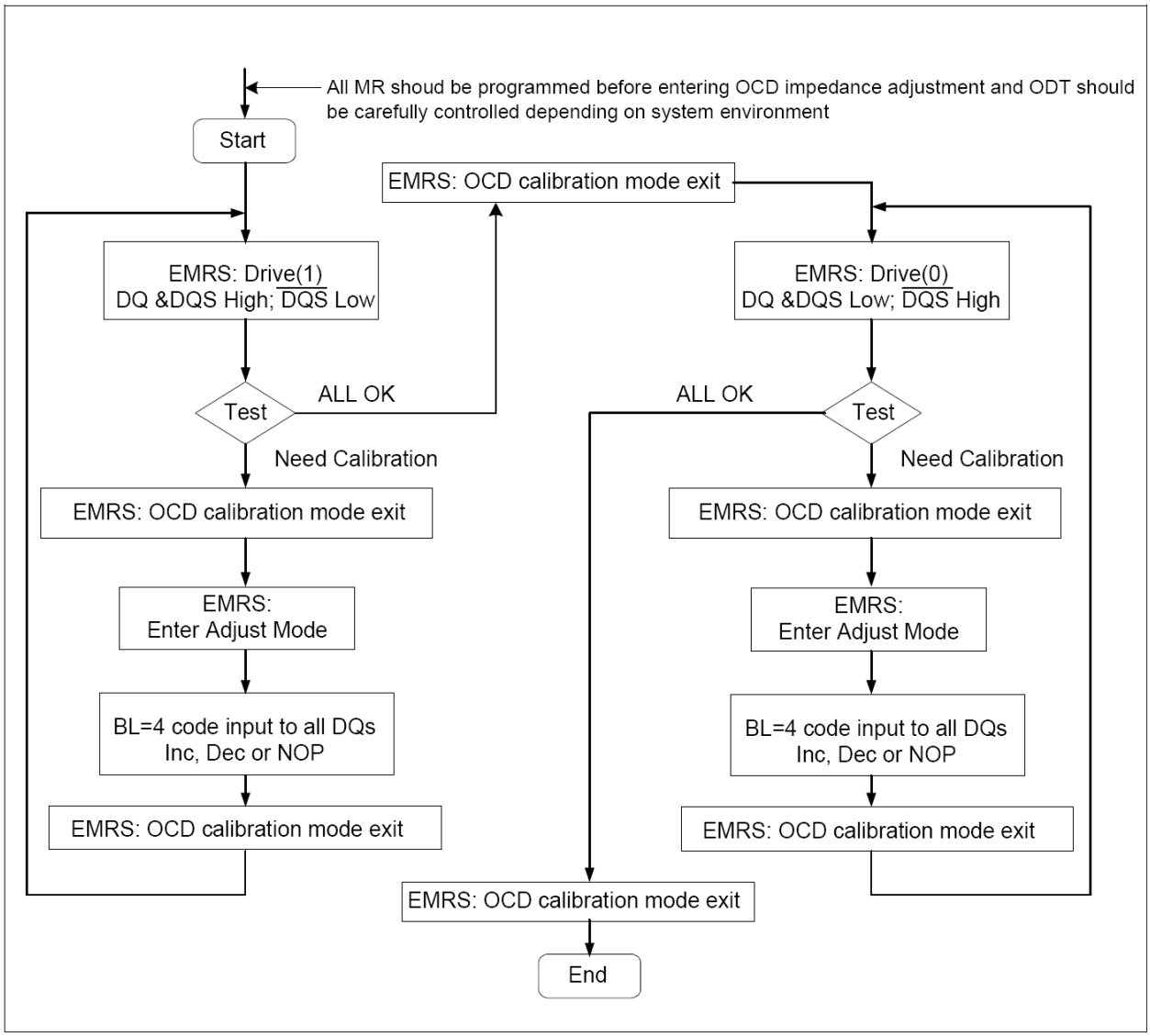


Figure 6 - OCD Impedance Adjustment Flow Chart

7.2.3.1. Extended Mode Register for OCD Impedance Adjustment

OCD impedance adjustment can be done using the following EMRS mode. In drive mode all outputs are driven out by DDR2 SDRAM. In Drive (1) mode, all DQ, DQS signals are driven HIGH and all /DQS signals are driven LOW. In Drive (0) mode, all DQ, DQS signals are driven LOW and all /DQS signals are driven HIGH. In adjust mode, BL = 4 of operation code data must be used. In case of OCD calibration default, output driver characteristics have a nominal impedance value of 18 Ohms during nominal temperature and voltage conditions. OCD applies only to normal full strength output drive setting defined by EMR (1) and if reduced strength is set, OCD default driver characteristics are not applicable. When OCD calibration adjust mode is used, OCD default output driver characteristics are not applicable. After OCD calibration is completed or driver strength is set to default, subsequent EMRS commands not intended to adjust OCD characteristics must specify A[9:7] as '000' in order to maintain the default or calibrated value.

A9	A8	A7	Operation
0	0	0	OCD calibration mode exit
0	0	1	Drive (1) DQ, DQS HIGH and /DQS LOW
0	1	0	Drive (0) DQ, DQS LOW and /DQS HIGH
1	0	0	Adjust mode
1	1	1	OCD calibration default

Table 1 - OCD Drive Mode Program

7.2.3.2. OCD Impedance Adjust

To adjust output driver impedance, controllers must issue the ADJUST EMRS command along with a 4 bit burst code to DDR2 SDRAM as in table 2. For this operation, Burst Length has to be set to BL = 4 via MRS command before activating OCD and controllers must drive the burst code to all DQs at the same time. DT0 in table 2 means all DQ bits at bit time 0, DT1 at bit time 1, and so forth. The driver output impedance is adjusted for all DDR2 SDRAM DQs simultaneously and after OCD calibration, all DQs and DQS's of a given DDR2 SDRAM will be adjusted to the same driver strength setting. The maximum step count for adjustment is 16 and when the limit is reached, further increment or decrement code has no effect. The default setting may be any step within the 16 step range. When Adjust mode command is issued, AL from previously set value must be applied.

4 bit burst code inputs to all DQs				Operation	
DT0	DT1	DT2	DT3	Pull-up driver strength	Pull-down driver strength
0	0	0	0	NOP (No operation)	NOP (No operation)
0	0	0	1	Increase by 1 step	NOP (No operation)
0	0	1	0	Decrease by 1 step	NOP (No operation)
0	1	0	0	NOP (No operation)	Increase by 1 step
1	0	0	0	NOP (No operation)	Decrease by 1 step
0	1	0	1	Increase by 1 step	Increase by 1 step
0	1	1	0	Decrease by 1 step	Increase by 1 step
1	0	0	1	Increase by 1 step	Decrease by 1 step
1	0	1	0	Decrease by 1 step	Decrease by 1 step
Other Combinations				Reserved	

Table 2 - OCD Adjust Mode Program

For proper operation of adjust mode, WL = RL - 1 = AL + CL - 1 clocks and tDS/tDH should be met as shown in Figure 7. For input data pattern for adjustment, DT0 - DT3 is a fixed order and is not affected by burst type (i.e., sequential or interleave).

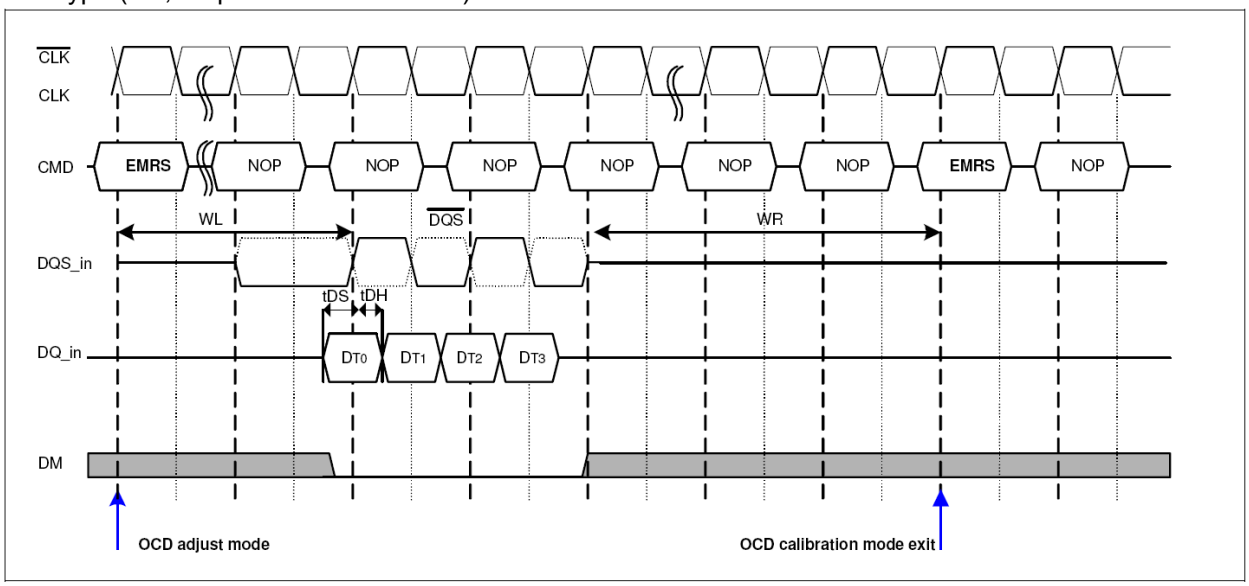


Figure 7 - OCD Adjust Mode

7.2.3.3. Drive Mode

Drive mode, both Drive (1) and Drive (0), is used for controllers to measure DDR2 SDRAM Driver impedance. In this mode, all outputs are driven out tOIT after “enter drive mode” command and all output drivers are turned-off tOIT after “OCD calibration mode exit” command as shown in Figure 8.

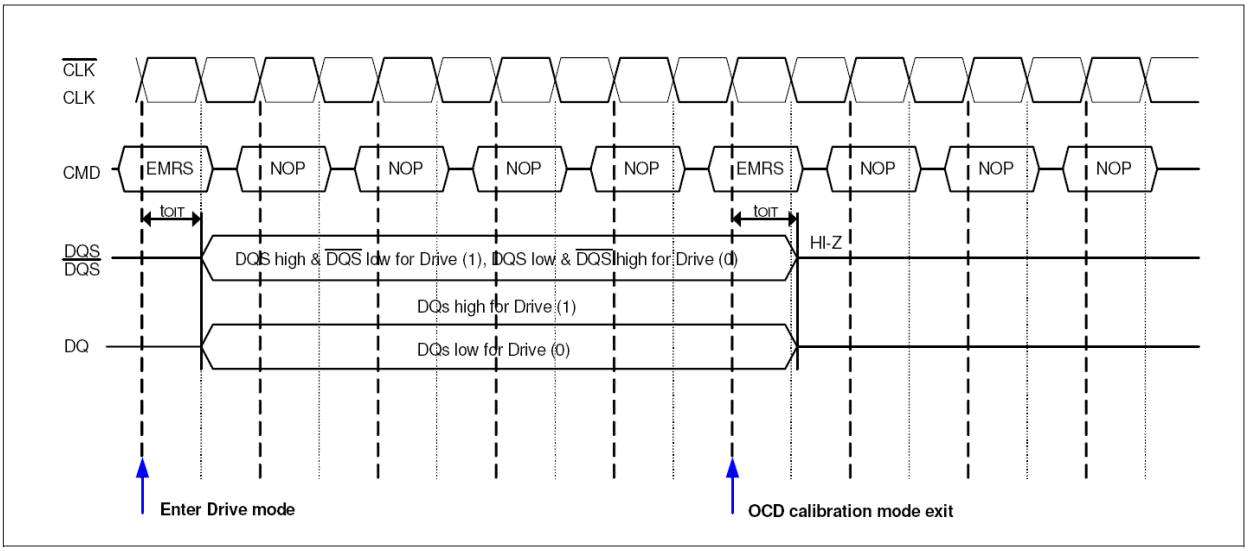
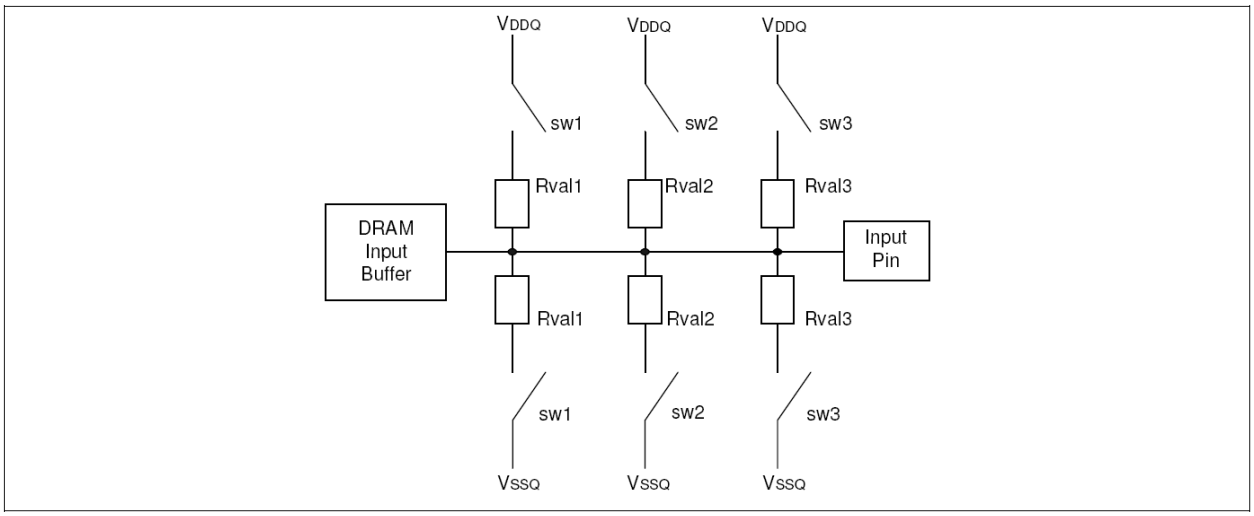


Figure 8 - OCD Drive Mode

7.2.4. On-Die Termination (ODT)

On-Die Termination (ODT) is a new feature on DDR2 components that allows a DRAM to turn on/off termination resistance for each DQ, UDQS/ /UDQS , LDQS/ /LDQS , UDM and LDM signal via the ODT control pin. /UDQS and LDQS are terminated only when enabled in the EMR (1) by address bit A10 = 0. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices.

The ODT function can be used for all active and standby modes. ODT is turned off and not supported in Self Refresh mode. (Example timing waveforms refer to 10.3, 10.4 ODT Timing for Active/Standby/Power Down Mode and 10.5, 10.6 ODT timing mode switch at entering/exiting power down mode diagram in Chapter 10)



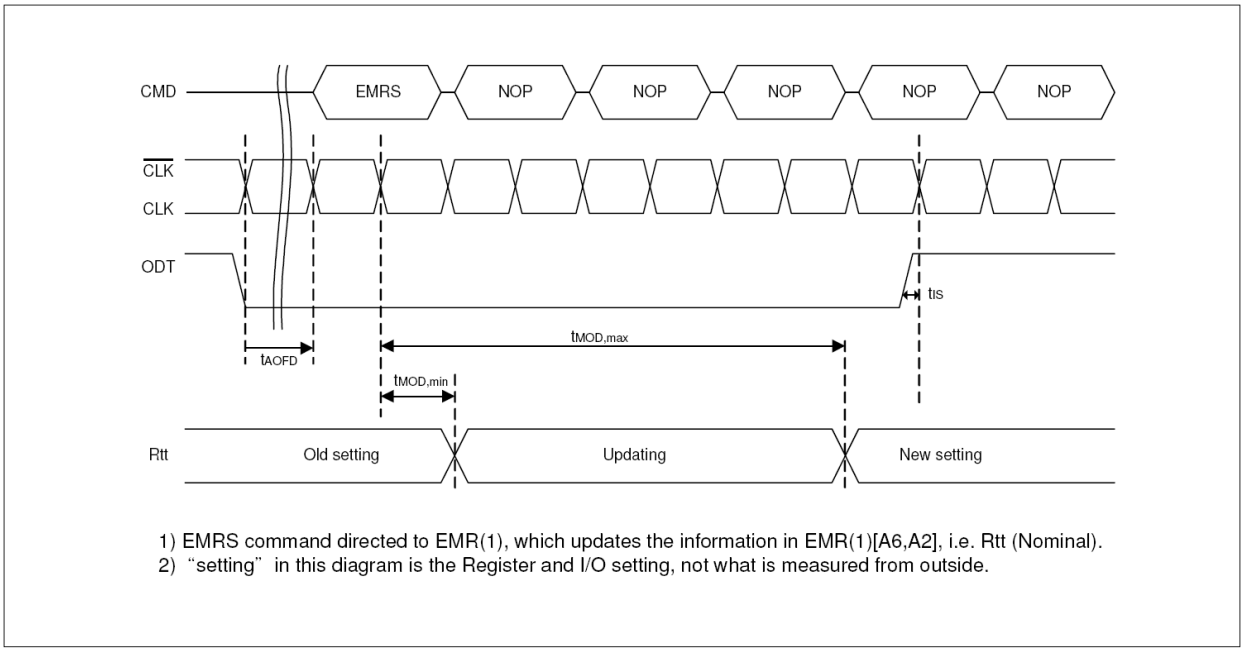
Switch (sw1, sw2, sw3) is enabled by ODT pin.
Selection among sw1, sw2, and sw3 is determined by “Rtt (nominal)” in EMR (1).
Termination included on all DQs, DM, DQS, DQS pins.

Figure 9 - Functional Representation of ODT

7.2.5. ODT related timings

7.2.5.1. MRS command to ODT update delay

During normal operation the value of the effective termination resistance can be changed with an EMRS command. The update of the Rtt setting is done between tMOD,min and tMOD,max, and CKE must remain HIGH for the entire duration of tMOD window for proper operation. The timings are shown in the following timing diagram.



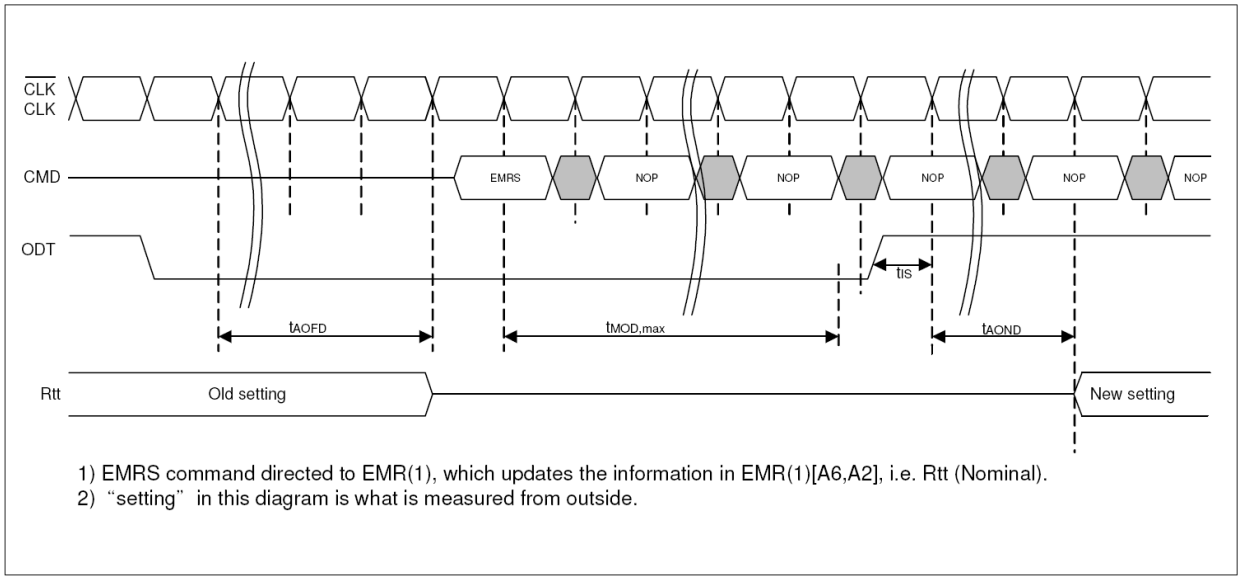
1) EMRS command directed to EMR(1), which updates the information in EMR(1)[A6,A2], i.e. Rtt (Nominal).
2) "setting" in this diagram is the Register and I/O setting, not what is measured from outside.

Figure 10 - ODT update delay timing - tMOD

However, to prevent any impedance glitch on the channel, the following conditions must be met.

- tAOFD must be met before issuing the EMRS command.
- ODT must remain LOW for the entire duration of tMOD window, until tMOD,max is met.

Now the ODT is ready for normal operation with the new setting, and the ODT signal may be raised again to turned on the ODT. Following timing diagram shows the proper Rtt update procedure.



1) EMRS command directed to EMR(1), which updates the information in EMR(1)[A6,A2], i.e. Rtt (Nominal).
2) "setting" in this diagram is what is measured from outside.

Figure 11 - ODT update delay timing - tMOD, as measured from outside

7.3. Command Function

7.3.1. Bank Activate Command

(/CS = "L", /RAS = "L", /CAS = "H", /WE = "H", BA0, BA1, BA2 = Bank, A0 to A12 be row address)

The Bank Activate command must be applied before any Read or Write operation can be executed. Immediately after the bank active command, the DDR2 SDRAM can accept a read or write command on the following clock cycle. If a Read/Write command is issued to a bank that has not satisfied the tRCDmin specification, then additive latency must be programmed into the device to delay when the Read/Write command is internally issued to the device. The additive latency value must be chosen to assure tRCDmin is satisfied. Additive latencies of 0, 1, 2, 3, 4, 5 and 6 are supported. Once a bank has been activated it must be precharged before another Bank Activate command can be applied to the same bank. The bank active and precharge times are defined as tRAS and tRP, respectively. The minimum time interval between successive Bank Activate commands to the same bank is determined by the RAS cycle time of the device (tRC). The minimum time interval between Bank Activate commands is tRRD.

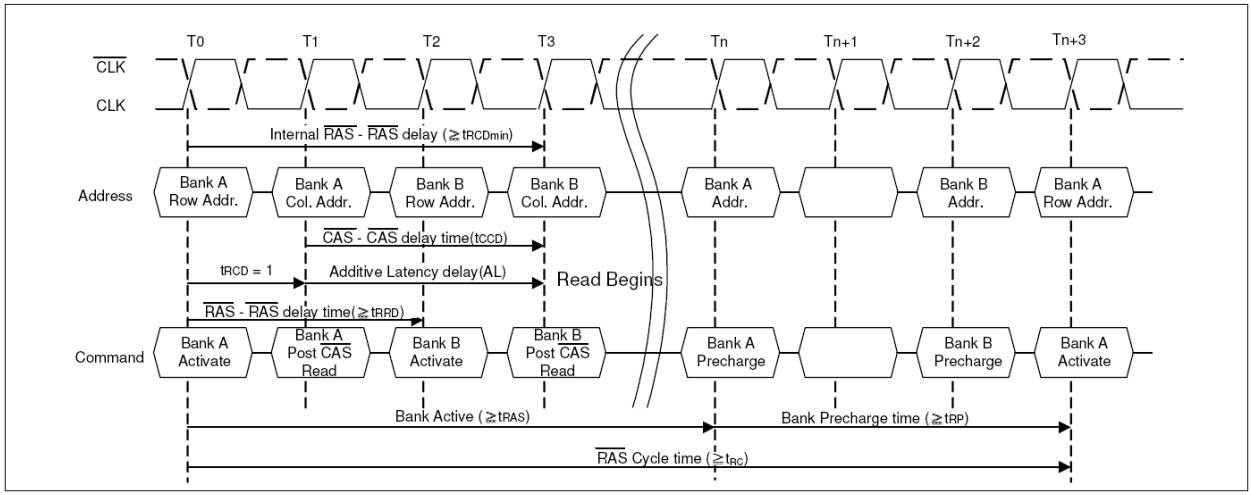


Figure 12 - Bank activate command cycle: tRCD = 3, AL = 2, tRP = 3, tRRD = 2, tCCD = 2

7.3.2. Read Command

(/CS = "L", /RAS = "H", /CAS = "L", /WE = "H", BA0, BA1, BA2 = Bank, A10 = "L", A0 to A9 = Column Address)

The READ command is used to initiate a burst read access to an active row. The value on BA0, BA1, BA2 inputs selects the bank, and the A0 to A9 address inputs determine the starting column address. The address input A10 determines whether or not Auto-precharge is used. If Auto-precharge is selected, the row being accessed will be precharged at the end of the READ burst; if Auto-precharge is not selected, the row will remain open for subsequent accesses.

7.3.3. Write Command

(/CS = "L", /RAS = "H", /CAS = "L", /WE = "L", BA0, BA1, BA2 = Bank, A10 = "L", A0 to A9 = Column Address)

The WRITE command is used to initiate a burst write access to an active row. The value on BA0, BA1, BA2 inputs selects the bank, and the A0 to A9 address inputs determine the starting column address. The address input A10 determines whether or not Auto-precharge is used. If Auto-precharge is selected, the row being accessed will be precharged at the end of the WRITE burst; if Auto-precharge is not selected, the row will remain open for subsequent accesses.

7.3.4. Burst Read with Auto-precharge Command

(/CS = "L", /RAS = "H", /CAS ="L", /WE = "H", BA0, BA1, BA2 = Bank, A10 = "H", A0 to A9 = Column Address)

If A10 is HIGH when a Read Command is issued, the Read with Auto-precharge function is engaged. The DDR2 SDRAM starts an Auto-precharge operation on the rising edge which is (AL + BL/2) cycles later than the read with AP command if tRAS(min) and tRTP(min) are satisfied.

7.3.5. Burst Write with Auto-precharge Command

(/CS = "L", /RAS = "H", /CAS = "L", /WE = "L", BA0, BA1, BA2 = Bank, A10 = "H", A0 to A9 = Column Address)

If A10 is HIGH when a Write Command is issued, the Write with Auto-precharge function is engaged. The DDR2 SDRAM automatically begins precharge operation after the completion of the burst write plus write recovery time (WR) programmed in the mode register.

7.3.6. Precharge All Command

(/CS = "L", /RAS = "L", /CAS = "H", /WE = "L", BA0, BA1, BA2 = Don't Care, A10 = "H", A0 to A9 and A11 to A12 = Don't Care)

The Precharge All command precharge all banks simultaneously. Then all banks are switched to the idle state.

7.3.7. Self Refresh Entry Command

(/CS = "L", /RAS = "L", /CAS = "L", /WE = "H", CKE = "L", BA0, BA1, BA2, A0 to A12 = Don't Care)

The Self Refresh command can be used to retain data, even if the rest of the system is powered down. When in the Self Refresh mode, the DDR2 SDRAM retains data without external clocking. The DDR2 SDRAM device has a built-in timer to accommodate Self Refresh operation. ODT must be turned off before issuing Self Refresh command, by either driving ODT pin LOW or using an EMRS command. Once the command is registered, CKE must be held LOW to keep the device in Self Refresh mode. The DLL is automatically disabled upon entering Self Refresh and is automatically enabled upon exiting Self Refresh. When the DDR2 SDRAM has entered Self Refresh mode, all of the external signals except CKE, are "Don't Care".

The clock is internally disabled during self refresh operation to save power. The user may change the external clock frequency or halt the external clock one clock after Self Refresh entry is registered; however, the clock must be restarted and stable before the device can exit self refresh operation.

7.3.8. Self Refresh Exit Command

(CKE = "H", /CS = "H" or CKE = "H", /CS = "L", /RAS = "H", /CAS = "H", /WE = "H", BA0, BA1, BA2, A0 to A12 = Don't Care)

The procedure for exiting Self Refresh requires a sequence of commands. First, the clock must be stable prior to CKE going back HIGH. Once Self Refresh Exit is registered, a delay of at least tXSNR must be satisfied before a valid command can be issued to the device to allow for any internal refresh in progress. CKE must remain HIGH for the entire Self Refresh exit period tXSRD for proper operation except for self refresh re-entry.

Upon exit from Self Refresh, the DDR2 SDRAM can be put back into Self Refresh mode after waiting at least tXSNR period and issuing one refresh command (refresh period of tRFC). NOP or Deselect commands must be registered on each positive clock edge during the Self Refresh exit interval tXSNR. ODT should be turned off during tXSRD.

The use of Self Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self Refresh mode. Upon exit from Self Refresh, the DDR2 SDRAM requires a minimum of one extra auto refresh command before it is put back into Self Refresh mode.

7.3.9. Refresh Command

(/CS = "L", /RAS = "L", /CAS = "L", /WE = "H", CKE = "H", BA0, BA1, BA2, A0 to A12 = Don't Care)

Refresh is used during normal operation of the DDR2 SDRAM. This command is non persistent, so it must be issued each time a refresh is required.

The refresh addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during an Auto Refresh command. The DDR2 SDRAM requires Auto Refresh cycles at an average periodic interval of tREFI (max.).

When the refresh cycle has completed, all banks of the DDR2 SDRAM will be in the precharged (idle) state. A delay between the auto refresh command (REF) and the next activate command or subsequent auto refresh command must be greater than or equal to the auto refresh cycle time (tRFC).

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight Refresh commands can be posted to any given DDR2 SDRAM, meaning that the maximum absolute interval between any Refresh command and the next Refresh command is 9 x tREFI.

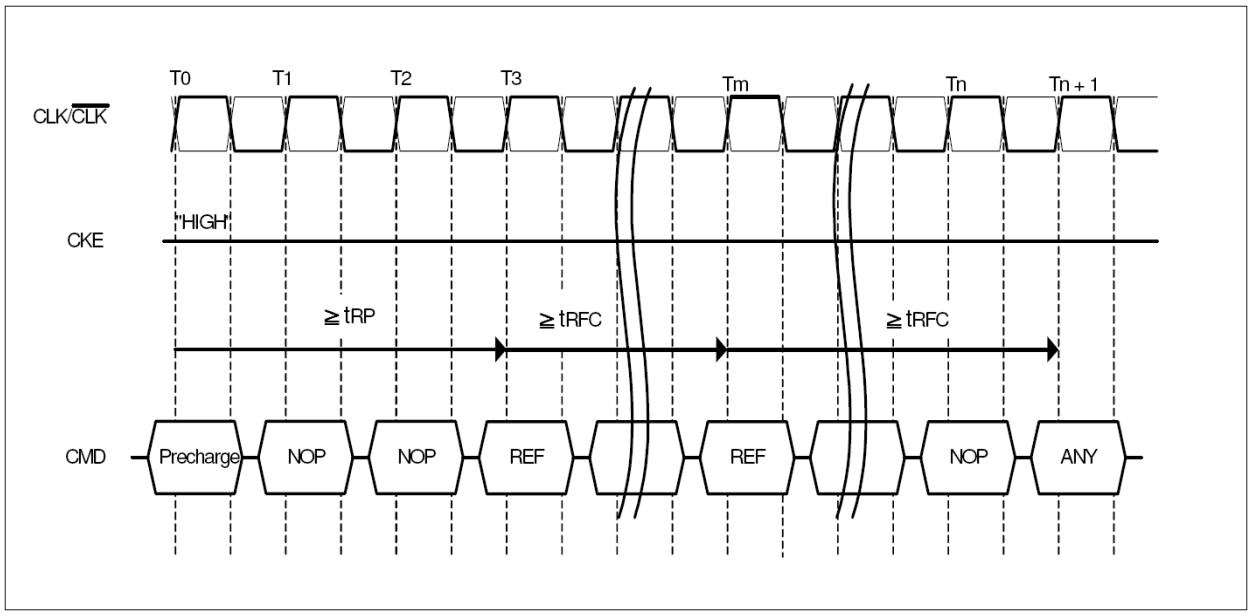


Figure 13 - Refresh command

7.3.10. No-Operation Command

(/CS = "L", /RAS = "H", /CAS = "H", /WE = "H", CKE, BA0, BA1, BA2, A0 to A12 = Don't Care)

The No-Operation command simply performs no operation (same command as Device Deselect).

7.3.11. Device Deselect Command

(/CS = "H", /RAS , /CAS , /WE , CKE, BA0, BA1, BA2, A0 to A12 = Don't Care)

The Device Deselect command disables the command decoder so that the /RAS , /CAS , /WE and Address inputs are ignored. This command is similar to the No-Operation command.

7.4. Read and Write access modes

The DDR2 SDRAM provides a fast column access operation. A single Read or Write Command will initiate a serial read or write operation on successive clock cycles. The boundary of the burst cycle is strictly restricted to specific segments of the page length.

The page length of 2048 is divided into 512 or 256 uniquely addressable boundary segments depending on burst length, 512 for 4 bit burst, 256 for 8 bit burst respectively. A 4-bit or 8-bit burst operation will occur entirely within one of the 512 or 256 groups beginning with the column address supplied to the device during the Read or Write Command (CA0-CA9, CA11). The second, third and fourth access will also occur within this group segment. However, the burst order is a function of the starting address, and the burst sequence.

A new burst access must not interrupt the previous 4 bit burst operation in case of BL = 4 setting. However, in case of BL = 8 setting, two cases of interrupt by a new burst access are allowed, one reads interrupted by a read, the other writes interrupted by a write with 4 bit burst boundary respectively. The minimum /CAS to /CAS delay is defined by tCCD, and is a minimum of 2 clocks for read or write cycles.

7.4.1. Posted /CAS

Posted /CAS operation is supported to make command and data bus efficient for sustainable bandwidths in DDR2 SDRAM. In this operation, the DDR2 SDRAM allows a /CAS read or write command to be issued immediately after the /RAS bank activate command (or any time during the /RAS - /CAS -delay time, tRCD, period). The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is controlled by the sum of AL and the CAS Latency (CL). Therefore if a user chooses to issue a Read/Write command before the tRCDmin, then AL (greater than 0) must be written into the EMR (1). The Write Latency (WL) is always defined as RL -1 (Read Latency -1) where Read Latency is defined as the sum of Additive Latency plus CAS Latency (RL = AL + CL). Read or Write operations using AL allow seamless bursts. (Example timing waveforms refer to 10.11 and 10.12 seamless burst read/write operation diagram in Chapter 10)

7.4.1.1. Examples of posted /CAS operation

Examples of a read followed by a write to the same bank where AL = 2 and where AL = 0 are shown in Figures 14 and 15, respectively.

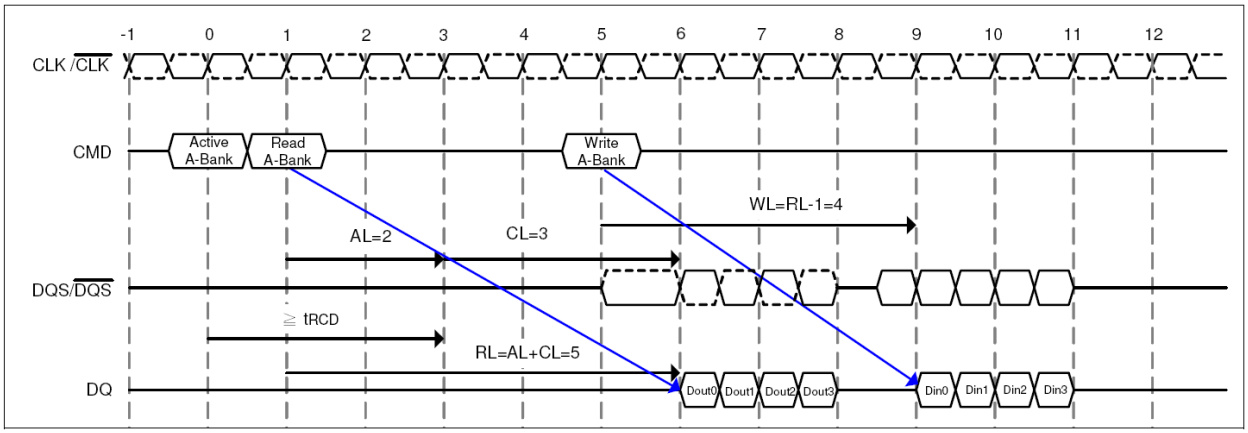


Figure 14 - Example 1: Read followed by a write to the same bank,
where AL = 2 and CL = 3, RL = (AL + CL) = 5, WL = (RL - 1) = 4, BL = 4

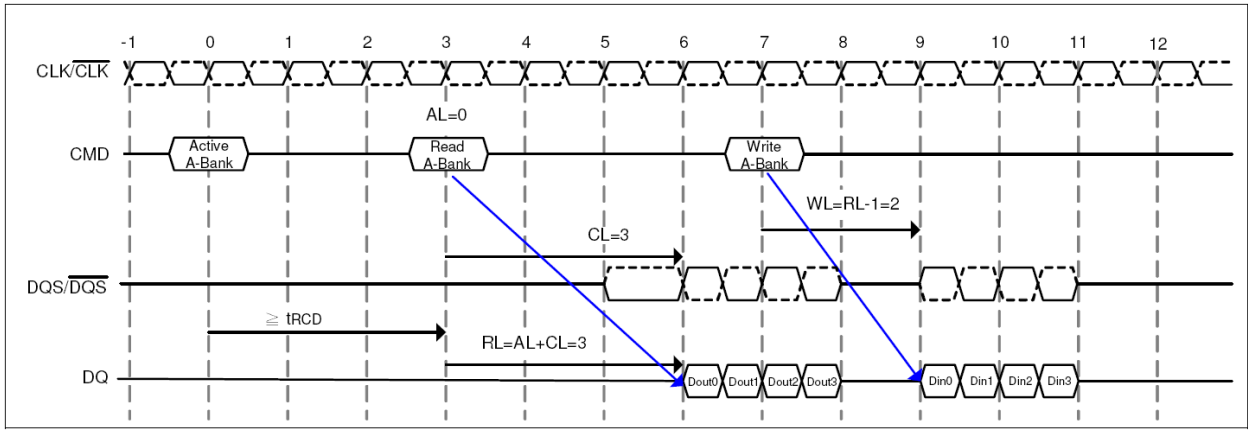


Figure 15 - Example 2: Read followed by a write to the same bank,
where AL = 0 and CL = 3, RL = (AL + CL) = 3, WL = (RL - 1) = 2, BL = 4

7.4.2. Burst mode operation

Burst mode operation is used to provide a constant flow of data to memory locations (write cycle), or from memory locations (read cycle). The parameters that define how the burst mode will operate are burst sequence and burst length. The DDR2 SDRAM supports 4 bit and 8 bit burst modes only. For 8 bit burst mode, full interleave address ordering is supported, however, sequential address ordering is nibble based for ease of implementation. The burst length is programmable and defined by MR A[2:0]. The burst type, either sequential or interleaved, is programmable and defined by MR [A3]. Seamless burst read or write operations are supported.

Unlike DDR1 devices, interruption of a burst read or writes cycle during BL = 4 mode operation is prohibited. However in case of BL = 8 mode, interruption of a burst read or write operation is limited to two cases, reads interrupted by a read, or writes interrupted by a write. (Example timing waveforms refer to 10.13 and 10.14 Burst read and write interrupt timing diagram in Chapter 10)

Therefore the Burst Stop command is not supported on DDR2 SDRAM devices.

Burst Length	Starting Address (A2 A1 A0)	Sequential Addressing (decimal)	Interleave Addressing (decimal)
4	x00	0, 1, 2, 3	0, 1, 2, 3
	x01	1, 2, 3, 0	1, 0, 3, 2
	x10	2, 3, 0, 1	2, 3, 0, 1
	x11	3, 0, 1, 2	3, 2, 1, 0
8	000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	001	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6
	010	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5
	011	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4
	100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	101	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2
	110	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1
	111	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0

Table 3 - Burst Length and Sequence

7.4.3. Burst read mode operation

Burst Read is initiated with a READ command. The address inputs determine the starting column address for the burst. The delay from the start of the command to when the data from the first cell appears on the outputs is equal to the value of the read latency (RL). The data strobe output (DQS) is driven LOW one clock cycle before valid data (DQ) is driven onto the data bus. The first bit of the burst is synchronized with the rising edge of the data strobe (DQS). Each subsequent data-out appears on the DQ pin in phase with the DQS signal in a source synchronous manner. The RL is equal to an additive latency (AL) plus CAS Latency (CL). The CL is defined by the Mode Register Set (MRS). The AL is defined by the Extended Mode Register EMR (1). (Example timing waveforms refer to 10.7 and 10.8 Data output (read) timing and Burst read operation diagram in Chapter 10)

7.4.4. Burst write mode operation

Burst Write is initiated with a WRITE command. The address inputs determine the starting column address for the burst. Write Latency (WL) is defined by a Read Latency (RL) minus one and is equal to (AL + CL -1); and is the number of clocks of delay that are required from the time the write command is registered to the clock edge associated to the first DQS strobe. A data strobe signal (DQS) should be driven LOW (preamble) nominally half clock prior to the WL. The first data bit of the burst cycle must be applied to the DQ pins at the first rising edge of the DQS following the preamble. The tDQSS specification must be satisfied for each positive DQS transition to its associated clock edge during write cycles. The subsequent burst bit data are issued on successive edges of the DQS until the burst length is completed, which is 4 or 8 bit burst. When the burst has finished, any additional data supplied to the DQ pins will be ignored. The DQ Signal is ignored after the burst write operation is complete. The time from the completion of the burst write to bank precharge is the write recovery time (WR). (Example timing waveforms refer to 10.9 and 10.10 Data input (write) timing and Burst write operation diagram in Chapter 10)

7.4.5. Write data mask

One write data mask (DM) pin for each 8 data bits (DQ) will be supported on DDR2 SDRAM, consistent with the implementation on DDR1 SDRAM. It has identical timings on write operations as the data bits, and though used in a unidirectional manner, is internally loaded identically to data bits to insure matched system timing. DM is not used during read cycles. (Example timing waveform refer to 10.15 Write operation with Data Mask diagram in Chapter 10)

7.5. Burst Interrupt

Read or Write burst interruption is prohibited for burst length of 4 and only allowed for burst length of 8 under the following conditions:

1. Read burst of 8 can only be interrupted by another Read command. Read burst interruption by Write or Precharge Command is prohibited.
2. Write burst of 8 can only be interrupted by another Write command. Write burst interruption by Read or Precharge Command is prohibited.
3. Read burst interrupt must occur exactly two clocks after the previous Read command. Any other Read burst interrupt timings are prohibited.
4. Write burst interrupt must occur exactly two clocks after the previous Write command. Any other Write burst interrupt timings are prohibited.
5. Read or Write burst interruption is allowed to any bank inside the DDR2 SDRAM.
6. Read or Write burst with Auto-precharge enabled is not allowed to interrupt.
7. Read burst interruption is allowed by a Read with Auto-precharge command.
8. Write burst interruption is allowed by a Write with Auto-precharge command.
9. All command timings are referenced to burst length set in the mode register. They are not referenced to the actual burst. For example below:
   - Minimum Read to Precharge timing is AL + BL/2 where BL is the burst length set in the mode register and not the actual burst (which is shorter because of interrupt).
   - Minimum Write to Precharge timing is WL + BL/ 2 + tWR, where tWR starts with the rising clock after the un-interrupted burst end and not from the end of the actual burst end.

(Example timing waveforms refer to 10.13 and 10.14 Burst read and write interrupt timing diagram in Chapter 10)

7.6. Precharge operation

The Precharge Command is used to precharge or close a bank that has been activated. The Precharge Command can be used to precharge each bank independently or all banks simultaneously. Three address bits A10, BA0 and BA1 and BA2 are used to define which bank to precharge when the command is issued.

A10	BA2	BA1	BA0	Precharge Bank(s)
L	L	L	L	Bank 0 only
L	L	L	H	Bank 1 only
L	L	H	L	Bank 2 only
L	L	H	H	Bank 3 only
L	H	L	L	Bank 4 only
L	H	L	H	Bank 5 only
L	H	H	L	Bank 6 only
L	H	H	H	Bank 7 only
H	Don't Care	Don't Care	Don't Care	All Banks

Table 4 - Bank selection for precharge by address bits

7.6.1. Burst read operation followed by precharge

Minimum Read to Precharge command spacing to the same bank = AL + BL/2 + max(RTP, 2) - 2 clks

For the earliest possible precharge, the precharge command may be issued on the rising edge which is "Additive Latency (AL) + BL/2 + max(RTP, 2) - 2 clocks" after a Read command. A new bank active (command) may be issued to the same bank after the RAS precharge time (tRP). A precharge command cannot be issued until tRAS is satisfied.

The minimum Read to Precharge spacing has also to satisfy a minimum analog time from the rising clock edge that initiates the last 4-bit prefetch of a Read to Precharge command. This time is called tRTP (Read to Precharge). For BL = 4 this is the time from the actual read (AL after the Read command) to Precharge command. For BL = 8 this is the time from AL + 2 clocks after the Read to the Precharge command. (Example timing waveforms refer to 10.16 to 10.20 Burst read operation followed by precharge diagram in Chapter 10)

7.6.2. Burst write operation followed by precharge

Minimum Write to Precharge Command spacing to the same bank = WL + BL/2 clks + tWR

For write cycles, a delay must be satisfied from the completion of the last burst write cycle until the Precharge Command can be issued. This delay is known as a write recovery time (tWR) referenced from the completion of the burst write to the precharge command. No Precharge command should be issued prior to the tWR delay. (Example timing waveforms refer to 10.21 to 10.22 Burst write operation followed by precharge diagram in Chapter 10)

7.7. Auto-precharge operation

Before a new row in an active bank can be opened, the active bank must be precharged using either the Precharge command or the Auto-precharge function. When a Read or a Write command is given to the DDR2 SDRAM, the /CAS timing accepts one extra address, column address A10, to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle. If A10 is LOW when the READ or WRITE command is issued, then normal Read or Write burst operation is executed and the bank remains active at the completion of the burst sequence. If A10 is HIGH when the Read or Write command is issued, then the Auto-precharge function is engaged. During Auto-precharge, a Read command will execute as normal with the exception that the active bank will begin to precharge on the rising edge which is CAS Latency (CL) clock cycles before the end of the read burst.

Auto-precharge is also implemented during Write commands. The precharge operation engaged by the Auto-precharge command will not begin until the last data of the burst write sequence is properly stored in the memory array.

This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon CAS Latency) thus improving system performance for random data access.

The /RAS lockout circuit internally delays the Precharge operation until the array restore operation has been completed (tRAS satisfied) so that the Auto-precharge command may be issued with any read or write command.

7.7.1. Burst read with Auto-precharge

If A10 is HIGH when a Read Command is issued, the Read with Auto-precharge function is engaged. The DDR2 SDRAM starts an Auto-precharge operation on the rising edge which is (AL + BL/2) cycles later from the Read with AP command if tRAS(min) and tRTP(min) are satisfied. (Example timing waveform refer to 10.23 Burst read operation with Auto-precharge diagram in Chapter 10)

If tRAS(min) is not satisfied at the edge, the start point of Auto-precharge operation will be delayed until tRAS(min) is satisfied.

If tRTP(min) is not satisfied at the edge, the start point of Auto-precharge operation will be delayed until tRTP(min) is satisfied.

In case the internal precharge is pushed out by tRTP, tRP starts at the point where tRTP ends (not at the next rising clock edge after this event). So for BL = 4 the minimum time from Read with Autoprecharge to the next Activate command becomes AL + RU{ (tRTP + tRP) / tCK } (Example timing waveform refer to 10.24 Burst read operation with Auto-precharge diagram in Chapter 10.), for BL = 8 the time from Read with Auto-precharge to the next Activate command is AL + 2 + RU{ (tRTP + tRP) / tCK }, where RU stands for “rounded up to the next integer”. In any event internal precharge does not start earlier than two clocks after the last 4-bit prefetch.

A new bank active command may be issued to the same bank if the following two conditions are satisfied simultaneously.

- The RAS precharge time (tRP) has been satisfied from the clock at which the Auto-precharge begins.
- The RAS cycle time (tRC) from the previous bank activation has been satisfied.

(Example timing waveforms refer to 10.25 to 10.26 Burst read with Auto-precharge followed by an activation to the same bank (tRC Limit) and (tRP Limit) diagram in Chapter 10)

7.7.2. Burst write with Auto-precharge

If A10 is HIGH when a Write Command is issued, the Write with Auto-Precharge function is engaged. The DDR2 SDRAM automatically begins precharge operation after the completion of the burst write plus write recovery time (WR) programmed in the mode register. The bank undergoing Autoprecharge from the completion of the write burst may be reactivated if the following two conditions are satisfied.

- The data-in to bank activate delay time (WR + tRP) has been satisfied.
- The /RAS cycle time (tRC) from the previous bank activation has been satisfied.

(Example timing waveforms refer to 10.27 to 10.28 Burst write with Auto-precharge (tRC Limit) and (WR + tRP) diagram in Chapter 10)

From Command	To Command	Minimum Delay between "From Command" to "To Command"	Unit	Notes
Read	Precharge (to same Bank as Read)	AL + BL/2 + max(RTP, 2) - 2	clks	1, 2
	Precharge All	AL + BL/2 + max(RTP, 2) - 2		1, 2
Read w/AP	Precharge (to same Bank as Read w/AP)	AL + BL/2 + max(RTP, 2) - 2		1, 2
	Precharge All	AL + BL/2 + max(RTP, 2) - 2		1, 2
Write	Precharge (to same Bank as Write)	WL + BL/2 + tWR		2
	Precharge All	WL + BL/2 + tWR		2
Write w/AP	Precharge (to same Bank as Write w/AP)	WL + BL/2 + tWR		2
	Precharge All	WL + BL/2 + tWR		2
Precharge	Precharge (to same Bank as Precharge)	1		2
	Precharge All	1		2
Precharge All	Precharge	1		2
	Precharge All	1		2

Table 5 - Precharge & Auto-precharge clarifications

Note:

1. RTP[cycles] = RU{ tRTP[nS] / tCK[nS] }, where RU stands for round up.
2. For a given bank, the precharge period should be counted from the latest precharge command, either one bank precharge or precharge all, issued to that bank. The precharge period is satisfied after tRP depending on the latest precharge command issued to that bank.

7.8. Refresh Operation

Two types of Refresh operation can be performed on the device: Auto Refresh and Self Refresh. By repeating the Auto Refresh cycle, each bank in turn refreshed automatically. The Refresh operation must be performed 8192 times (rows) within 64mS. The period between the Auto Refresh command and the next command is specified by tRFC.

Self Refresh mode enters issuing the Self Refresh command (CKE asserted "LOW") while all banks are in the idle state. The device is in Self Refresh mode for as long as CKE held "LOW". In the case of 8192 burst Auto Refresh commands, 8192 burst Auto Refresh commands must be performed within 7.8 µS before entering and after exiting the Self Refresh mode. In the case of distributed Auto Refresh commands, distributed auto refresh commands must be issued every 7.8 µS and the last distributed Auto Refresh commands must be performed within 7.8 µS before entering the self refresh mode. After exiting from the Self Refresh mode, the refresh operation must be performed within 7.8 µS. In Self Refresh mode, all input/output buffers are disable, resulting in lower power dissipation (except CKE buffer). (Example timing waveform refer to 10.29 Self Refresh diagram in Chapter 10)

7.9. Power Down Mode

Power-down is synchronously entered when CKE is registered LOW, along with NOP or Deselect command. CKE is not allowed to go LOW while mode register or extended mode register command time, or read or write operation is in progress. CKE is allowed to go LOW while any other operation such as row activation, Precharge or Auto-precharge or Auto Refresh is in progress, but power down IDD specification will not be applied until finishing those operations.

The DLL should be in a locked state when power-down is entered. Otherwise DLL should be reset after exiting power-down mode for proper read operation.

7.9.1. Power Down Entry

Two types of Power Down Mode can be performed on the device: Precharge Power Down Mode and Active Power Down Mode.

If power down occurs when all banks are idle, this mode is referred to as Precharge Power Down; if power down occurs when there is a row active in any bank, this mode is referred to as Active Power Down. Entering power down deactivates the input and output buffers, excluding CLK, CLK , ODT and CKE. Also the DLL is disabled upon entering Precharge Power Down or slow exit Active Power Down, but the DLL is kept enabled during fast exit Active Power Down.

In power down mode, CKE LOW and a stable clock signal must be maintained at the inputs of the DDR2 SDRAM, and ODT should be in a valid state but all other input signals are “Don’t Care”. CKE LOW must be maintained until tCKE has been satisfied. Maximum power down duration is limited by the refresh requirements of the device, which allows a maximum of 9 x tREFI if maximum posting of REF is utilized immediately before entering power down. (Example timing waveforms refer to 10.30 to 10.31 Active and Precharged Power Down Mode Entry and Exit diagram in Chapter 10)

7.9.2. Power Down Exit

The power-down state is synchronously exited when CKE is registered HIGH (along with a NOP or Deselect command). CKE high must be maintained until tCKE has been satisfied. A valid, executable command can be applied with power-down exit latency, tXP, tXARD, or tXARDS, after CKE goes HIGH. Power-down exit latency is defined at AC Characteristics table of this data sheet.

7.10. Input clock frequency change during precharge power down

DDR2 SDRAM input clock frequency can be changed under following condition:

DDR2 SDRAM is in precharged power down mode. ODT must be turned off and CKE must be at logic LOW level. A minimum of 2 clocks must be waited after CKE goes LOW before clock frequency may change. SDRAM input clock frequency is allowed to change only within minimum and maximum operating frequency specified for the particular speed grade. During input clock frequency change, ODT and CKE must be held at stable LOW levels.

Once input clock frequency is changed, stable new clocks must be provided to DRAM before precharge power down may be exited and DLL must be RESET via MRS command after precharge power down exit. Depending on new clock frequency an additional MRS or EMRS command may need to be issued to appropriately set the WR, CL etc…

During DLL re-lock period, ODT must remain off. After the DLL lock time, the DRAM is ready to operate with new clock frequency. (Example timing waveform refer to 10.32 Clock frequency change in precharge Power Down mode diagram in Chapter 10)

8. OPERATION MODE

8.1. Command Truth Table

COMMAND	CKE		BA2 BA1 BA0	A12 A11	A10	A9-A0	/CS	/RAS	/CAS	/WE	NOTES
	Previous Cycle	Current Cycle									
Bank Activate	H	H	BA	Row Address			L	L	H	H	1,2
Single Bank Precharge	H	H	BA	X	L	X	L	L	H	L	1,2
Precharge All Banks	H	H	X	X	H	X	L	L	H	L	1
Write	H	H	BA	Column	L	Column	L	H	L	L	1,2,3
Write with Auto-precharge	H	H	BA	Column	H	Column	L	H	L	L	1,2,3
Read	H	H	BA	Column	L	Column	L	H	L	H	1,2,3
Read with Auto-precharge	H	H	BA	Column	H	Column	L	H	L	H	1,2,3
(Extended) Mode Register Set	H	H	BA	OP Code			L	L	L	L	1,2
No Operation	H	X	X	X	X	X	L	H	H	H	1
Device Deselect	H	X	X	X	X	X	H	X	X	X	1
Refresh	H	H	X	X	X	X	L	L	L	H	1
Self Refresh Entry	H	L	X	X	X	X	L	L	L	H	1,4
Self Refresh Exit	L	H	X	X	X	X	H	X	X	X	1,4,5
							L	H	H	H	
Power Down Mode Entry	H	L	X	X	X	X	H	X	X	X	1,6
							L	H	H	H	
Power Down Mode Exit	L	H	X	X	X	X	H	X	X	X	1,6
							L	H	H	H	

Note:

1. All DDR2 SDRAM commands are defined by states of /CS , /RAS , /CAS , /WE and CKE at the rising edge of the clock.
2. Bank addresses BA [2:0] determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.
3. Burst reads or writes at BL = 4 can not be terminated or interrupted. See Burst Interrupt in Chapter 7.5 for details.
4. VREF must be maintained during Self Refresh operation.
5. Self Refresh Exit is asynchronous.
6. The Power Down does not perform any refresh operations. The duration of Power Down Mode is therefore limited by the refresh requirements outlined in Chapter 7.9.

8.2. Clock Enable (CKE) Truth Table for Synchronous Transitions

CURRENT STATE[2]	CKE		COMMAND (N)[3] /RAS , /CAS , /WE , /CS	ACTION (N)[3]	NOTES
	Previous Cycle[1] (N-1)	Current Cycle[1] (N)			
Power Down	L	L	X	Maintain Power Down	11,12,13
	L	H	DESELECT or NOP	Power Down Exit	4,8,11,12
Self Refresh	L	L	X	Maintain Power Down	11,13,14
	L	H	DESELECT or NOP	Self Refresh Exit	4,5,9,14
Bank(s) Active	H	L	DESELECT or NOP	Active Power Down Entry	4,8,10,11,12
All Banks Idle	H	L	DESELECT or NOP	Precharge Power Down Entry	4,8,10,11,12
	H	L	REFRESH	Self Refresh Entry	6,9,11,12
	H	H	Refer to the Command Truth Table		7

Note:

1. CKE (N) is the logic state of CKE at clock edge N; CKE (N–1) was the state of CKE at the previous clock edge.
2. Current state is the state of the DDR2 SDRAM immediately prior to clock edge N.
3. COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N).
4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
5. On Self Refresh Exit DESELECT or NOP commands must be issued on every clock edge occurring during the tXSNR period. Read commands may be issued only after tXSRD (200 clocks) is satisfied.
6. Self Refresh mode can only be entered from the All Banks Idle state.
7. Must be a legal command as defined in the Command Truth Table.
8. Valid commands for Power Down Entry and Exit are NOP and DESELECT only.
9. Valid commands for Self Refresh Exit are NOP and DESELECT only.
10. Power Down and Self Refresh can not be entered while Read or Write operations, (Extended) Mode Register Set operations or Precharge operations are in progress. See Chapter 7.9 "Power Down Mode" and Chapter 7.3.7/7.3.8 "Self Refresh Entry/Exit Command" for a detailed list of restrictions.
11. tCKEmin of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of tIS + 2 x tCK + tIH.
12. The Power Down does not perform any refresh operations. The duration of Power Down Mode is therefore limited by the refresh requirements outlined in Chapter 7.9.
13. ”X” means “don’t care (including floating around VREF)” in Self Refresh and Power Down. However ODT must be driven high or low in Power Down if the ODT function is enabled (Bit A2 or A6 set to “1” in EMR (1)).
14. VREF must be maintained during Self Refresh operation.

8.3. Data Mask (DM) Truth Table

FUNCTION	DM	DQS	NOTE
Write enable	L	Valid	1
Write inhibit	H	X	1

Note:

1. Used to mask write data, provided coincident with the corresponding data.

8.4. Function Truth Table

CURRENT STATE	/CS	/RAS	/CAS	/WE	ADDRESS	COMMAND	ACTION	NOTE
Idle	H	X	X	X	X	DSL	NOP or Power down	
	L	H	H	H	X	NOP	NOP or Power down	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	1
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	1
	L	L	H	H	BA, RA	ACT	Row activating	
	L	L	H	L	BA, A10	PRE/PREA	Precharge/ Precharge all banks	
	L	L	L	H	X	AREF/SELF	Auto Refresh or Self Refresh	2
	L	L	L	L	Op-Code	MRS/EMRS	Mode/Extended register accessing	2
Banks Active	H	X	X	X	X	DSL	NOP	
	L	H	H	H	X	NOP	NOP	
	L	H	L	H	BA, CA, A10	READ/READA	Begin read	
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Begin write	
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10	PRE/PREA	Precharge/ Precharge all banks	
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Read	H	X	X	X	X	DSL	Continue burst to end	
	L	H	H	H	X	NOP	Continue burst to end	
	L	H	L	H	BA, CA, A10	READ/READA	Burst interrupt	1,3
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	1
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL	1
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Write	H	X	X	X	X	DSL	Continue burst to end	
	L	H	H	H	X	NOP	Continue burst to end	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	1
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Burst interrupt	1,3
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL	1
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	

Function Truth Table, continued

CURRENT STATE	/CS	/RAS	/CAS	/WE	ADDRESS	COMMAND	ACTION	NOTE
Read with Auto-precharge	H	X	X	X	X	DSL	Continue burst to end	
	L	H	H	H	X	NOP	Continue burst to end	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	1
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	1
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL	1
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Write with Auto-precharge	H	X	X	X	X	DSL	Continue burst to end	
	L	H	H	H	X	NOP	Continue burst to end	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	1
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	1
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL	1
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Precharge	H	X	X	X	X	DSL	NOP-> Idle after tRP	
	L	H	H	H	X	NOP	NOP-> Idle after tRP	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	1
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	1
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10	PRE/PREA	NOP-> Idle after tRP	1
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Row Activating	H	X	X	X	X	DSL	NOP-> Row active after tRCD	
	L	H	H	H	X	NOP	NOP-> Row active after tRCD	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	1
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	1
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL	1
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	

Function Truth Table, continued

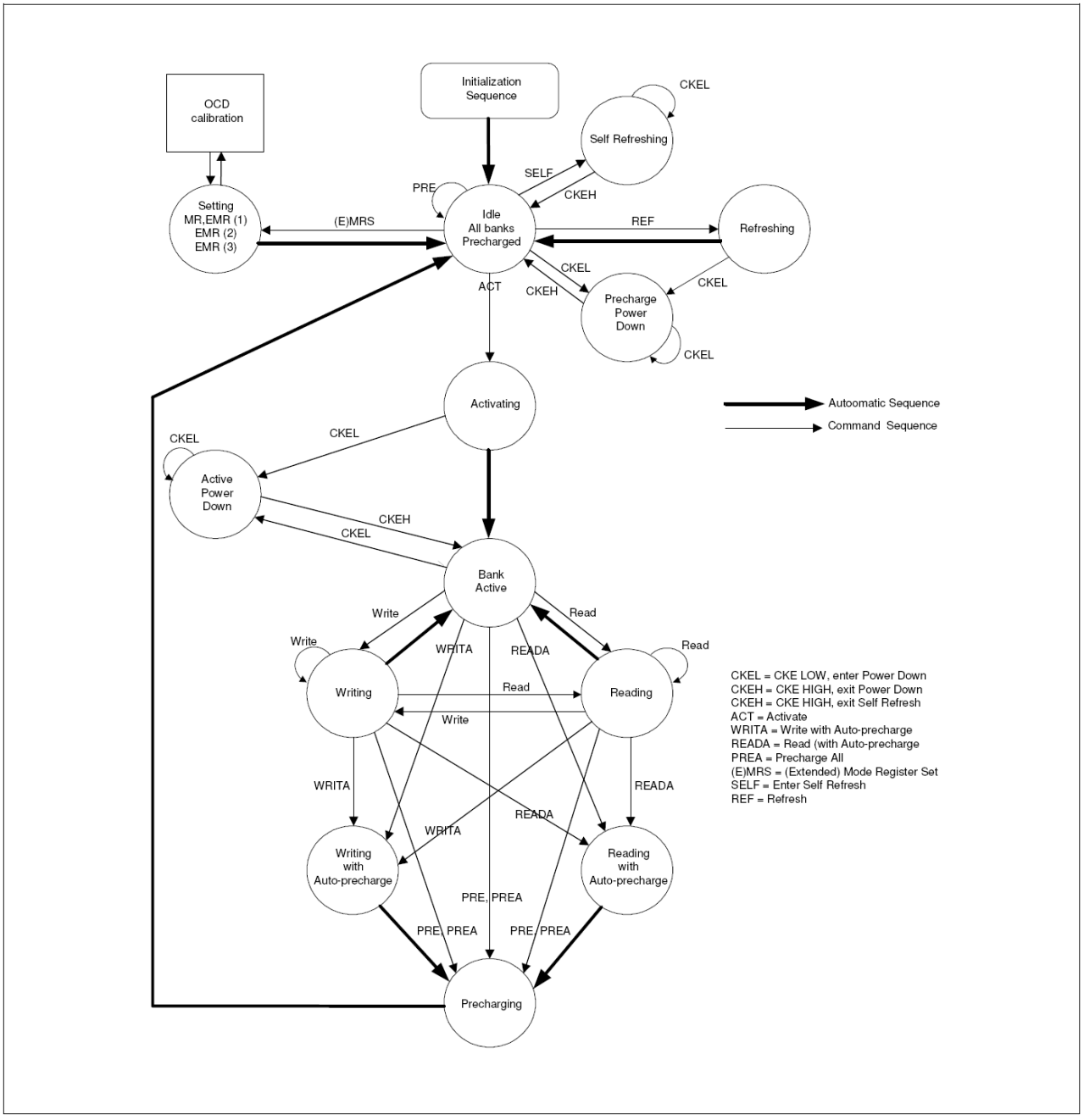
CURRENT STATE	/CS	/RAS	/CAS	/WE	ADDRESS	COMMAND	ACTION	NOTE
Write Recovering	H	X	X	X	X	DSL	NOP-> Bank active after tWR	
	L	H	H	H	X	NOP	NOP-> Bank active after tWR	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	1
	L	H	L	L	BA, CA, A10	WRIT/WRITA	New write	
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL	1
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Write Recovering with Auto-precharge	H	X	X	X	X	DSL	NOP-> Precharge after tWR	
	L	H	H	H	X	NOP	NOP-> Precharge after tWR	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	1
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	1
	L	L	H	H	BA, RA	ACT	ILLEGAL	1
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL	1
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Refreshing	H	X	X	X	X	DSL	NOP-> Idle after tRC	
	L	H	H	H	X	NOP	NOP-> Idle after tRC	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL	
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	
Mode Register Accessing	H	X	X	X	X	DSL	NOP-> Idle after tMRD	
	L	H	H	H	X	NOP	NOP-> Idle after tMRD	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	
	L	L	H	L	BA, A10	PRE/PREA	ILLEGAL	
	L	L	L	H	X	AREF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS/EMRS	ILLEGAL	

Note:

1. This command may be issued for other banks, depending on the state of the banks.
2. All banks must be in "IDLE".
3. Read or Write burst interruption is prohibited for burst length of 4 and only allowed for burst length of 8. Burst read/write can only be interrupted by another read/write with 4 bit burst boundary. Any other case of read/write interrupt is not allowed.

Remark: H = High level, L = Low level, X = High or Low level (Don't Care), V = Valid data.

8.5. Simplified Stated Diagram



9. ELECTRICAL CHARACTERISTICS

9.1. Absolute Maximum Ratings

PARAMETER	SYMBOL	RATING	UNIT	NOTES
Voltage on VDD pin relative to VSS	VDD	-1.0 ~ 2.3	V	1,2
Voltage on VDDQ pin relative to VSS	VDDQ	-0.5 ~ 2.3	V	1,2
Voltage on VDDL pin relative to VSS	VDDL	-0.5 ~ 2.3	V	1,2
Voltage on any pin relative to VSS	VIN, VOUT	-0.5 ~ 2.3	V	1,2
Storage Temperature	TSTG	-55 ~ 100	°C	1,2,3

Note:

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. When VDD and VDDQ and VDDL are less than 500mV; VREF may be equal to or less than 300mV.
3. Storage temperature is the case surface temperature on the center/top side of the DRAM.

9.2. Operating Temperature Condition

PARAMETER	SYMBOL	RATING	UNIT	NOTES
Operating Temperature	TOPR	0 ~ 85	°C	1,2,3

Note:

1. Operating Temperature is the case surface temperature on the center/top side of the DRAM.
2. Supporting 0 ~ 85°C with full JEDEC AC and DC specifications.
3. Supporting 0 ~ 85 °C and being able to extend to 95 °C with doubling Auto Refresh commands in frequency to a 32 mS period (tREFI = 3.9 µS) and to enter to Self Refresh mode at this high temperature range via A7 "1" on EMR (2).

9.3. Recommended DC Operating Conditions

(0℃ ≦ TCASE ≦ 85℃ for -18/-25/-3, VDD, VDDQ = 1.8V ± 0.1V)

SYM	PARAMETER	MIN	TYP	MAX	UNIT	NOTES
VDD	Supply Voltage	1.7	1.8	1.9	V	1
VDDL	Supply Voltage for DLL	1.7	1.8	1.9	V	5
VDDQ	Supply Voltage for Output	1.7	1.8	1.9	V	1,5
VREF	Input Reference Voltage	0.49 x VDDQ	0.5 x VDDQ	0.51 x VDDQ	V	2,3
VTT	Termination Voltage (System)	VREF - 0.04	VREF	VREF + 0.04	V	4

Note:

1. There is no specific device VDD supply voltage requirement for SSTL_18 compliance. However under all conditions VDDQ must than or equal to VDD.
2. The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about 0.5 x VDDQ of the transmitting device and VREF is expected to track variations in VDDQ.
3. Peak to peak AC noise on VREF may not exceed +/-2 % VREF(dc).
4. VTT of transmitting device must track VREF of receiving device.
5. VDDQ tracks with VDD, VDDL tracks with VDD. AC parameters are measured with VDD, VDDQ and VDDDL tied together.

9.4. ODT DC Electrical Characteristics

(0℃ ≦ TCASE ≦ 85℃ for -18/-25/-3, VDD, VDDQ = 1.8V ± 0.1V)

PARAMETER / CONDITION	SYM	MIN	NOM	MAX	UNIT	NOTES
Rtt effective impedance value for EMRS(A6,A2)=0,1; 75Ω	Rtt1(eff)	60	75	90	Ω	1
Rtt effective impedance value for EMRS(A6,A2)=1,0; 150Ω	Rtt2(eff)	120	150	180	Ω	5
Rtt effective impedance value for EMRS(A6,A2)=1,1; 50Ω	Rtt3(eff)	40	50	60	Ω	1,5
Deviation of VM with respect to VDDQ/2	△VM	-6		+6	%	2,3

Note:

1. Test condition for Rtt measurements.
2. Optional for DDR2-667.

Measurement Definition for Rtt(eff):

Apply VIH (ac) and VIL (ac) to test pin separately, then measure current I(VIH (ac)) and I(VIL (ac)) respectively. VIH (ac), VIL (ac), and VDDQ values defined in SSTL_18.

$$Rtt(eff) = (VIH(ac) – VIL(ac)) /(I(VIHac) – I(VILac))$$

Measurement Definition for △VM:

Measure voltage (VM) at test pin (midpoint) with no load.

$$\triangle VM = ((2 \times Vm / VDDQ) – 1) \times 100\%$$

9.5. Input DC Logic Level

(0℃ ≦ TCASE ≦ 85℃ for -18/-25/-3, VDD, VDDQ = 1.8V ± 0.1V)

PARAMETER	SYM	MIN	MAX	UNIT
DC input logic HIGH	VIH(dc)	VREF + 0.125	VDDQ + 0.3	V
DC input logic LOW	VIL(dc)	-0.3	VREF - 0.125	V

9.6. Input AC Logic Level

(0℃ ≦ TCASE ≦ 85℃ for -18/-25/-3, VDD, VDDQ = 1.8V ± 0.1V)

PARAMETER	SYM	-18		-25 / -3		UNIT
		MIN	MAX	MIN	MAX	
AC input logic HIGH	VIH(ac)	VREF + 0.200	-	VREF + 0.200	VSSQ + VPEAK-	V
AC input logic LOW	VIL(ac)	-	VREF - 0.200	VSSQ - VPEAK	VREF - 0.200	V

9.7. Capacitance

SYM	PARAMETER	MIN	MAX	UNIT
CCK	Input Capacitance , CLK and /CLK	1.0	2.0	pF
CDCK	Input Capacitance delta , CLK and /CLK	-	0.25	pF
CI	input Capacitance, all other input-only pins	1.0	2.0	pF
CDI	Input Capacitance delta, all other input-only pins	-	0.25	pF
CIO	Input/output Capacitance, DQ, LDM, UDM, LDQS, /LDQS , UDQS, /UDQS	2.5	3.5	pF
CDIO	Input/output Capacitance delta, DQ, LDM, UDM, LDQS, /LDQS , UDQS, /UDQS	-	0.5	pF

9.8. Leakage and Output Buffer Characteristics

SYM	PARAMETER	MIN	MAX	UNIT	NOTES
IIL	Input Leakage Current (0V≦VIN≦VDD)	-2	2	uA	1
IOL	Output Leakage Current (Output disabled, 0V≦VOUT≦VDDQ)	-5	5	uA	2
VOH	Minimum Required Output Pull-up	VTT + 0.603	-	V	
VOL	Maximum Required Output Pull-down	-	VTT – 0.603	V	
IOH(dc)	Output Minimum Source DC Current	-13.4	-	mA	3,5
IOL(dc)	Output Minimum Sink DC Current	13.4	-	mA	4,5

Note:

1. All other pins not under test = 0 V.
2. DQ, LDQS, /LDQS , UDQS, /UDQS are disabled and ODT is turned off.
3. VDDQ = 1.7 V; VOUT = 1.42 V. (VOUT - VDDQ)/IOH must be less than 21 C for values of VOUT between VDDQ and VDDQ -0.28V.
4. VDDQ = 1.7 V; VOUT = 0.28V. VOUT/IOL must be less than 21 C for values of VOUT between 0 V and 0.28V.
5. The values of IOH(dc) and IOL(dc) are based on the conditions given in Notes 3 and 4. They are used to test drive current capability to ensure VIHmin plus a noise margin and VILmax minus a noise margin are delivered to an SSTL_18 receiver.

9.9. DC Characteristics

9.9.1. DC Characteristics for -18/-25/-3 speed grades

SYM	CONDITIONS		-18 MAX	-25 MAX	-3 MAX	UNIT	NOTE
IDD0	**Operating Current - One Bank Active-Precharge** tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address and control inputs are SWITCHING; Databus inputs are SWITCHING.		96	82	78	mA	1,2,3, 4,5,6
IDD1	**Operating Current - One Bank Active-Read-Precharge** IOUT = 0 mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD), tRCD=tRCD(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address and control inputs are SWITCHING; Data bus inputs are SWITCHING.		98	87	83	mA	1,2,3, 4,5,6
IDD2P	**Precharge Power-Down Current** All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address inputs are STABLE; Data Bus inputs are FLOATING.		4	7	6	mA	1,2,3, 4,5,6
IDD2N	**Precharge Standby Current** All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address inputs are SWITCHING; Data bus inputs are SWITCHING.		62	52	47	mA	1,2,3, 4,5,6
IDD2Q	**Precharge Quiet Standby Current** All banks idle; tCK = tCK(IDD); CKE is HIGH, /CS is HIGH; Other control and address inputs are STABLE; Data bus inputs are FLOATING.		58	47	43	mA	1,2,3, 4,5,6
IDD3P	**Active Power-Down Current** All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address inputs are STABLE; Data bus inputs are FLOATING.	Fast PDN Exit MRS(12) = 0	24	21	19	mA	1,2,3, 4,5,6
		Slow PDN Exit MRS(12) = 1	9	7	6	mA	1,2,3, 4,5,6
IDD3N	**Active Standby Current** All banks open; tCK = tCK(IDD); tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Other control and address inputs are SWITCHING; Data bus inputs are SWITCHING.		68	57	52	mA	1,2,3, 4,5,6

IDD4R	**Operating Burst Read Current** All banks open, Continuous burst reads, IOUT = 0 mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD); tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address inputs are SWITCHING; Data Bus inputs are SWITCHING.	171	142	127	mA	1,2,3, 4,5,6
IDD4W	**Operating Burst Write Current** All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD); tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, /CS is HIGH between valid commands; Address inputs are SWITCHING; Data Bus inputs are SWITCHING.	187	156	138	mA	1,2,3, 4,5,6
IDD5B	**Burst Refresh Current** tCK = tCK(IDD); Refresh command every tRFC(IDD) interval; CKE is HIGH, CS is HIGH between valid commands; Other control and address inputs are SWITCHING; Data bus inputs are SWITCHING.	168	157	151	mA	1,2,3, 4,5,6
IDD6	**Self Refresh Current** CKE≦0.2 V, external clock off, CLK and CLK at 0 V; Other control and address inputs are FLOATING; Data bus inputs are FLOATING.	9	9	9	mA	1,2,3, 4,5,6
IDD7	**Operating Bank Interleave Read Current** All bank interleaving reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = tRCD(IDD) - 1 x tCK(IDD); tCK = tCK(IDD), tRC = tRC(IDD), tRRD = tRRD(IDD), tRCD = tRCD(IDD); CKE is HIGH, CS is HIGH between valid commands; Address bus inputs are STABLE during deselects; Data Bus inputs are SWITCHING.	224	214	194	mA	1,2,3, 4,5,6

Note:

1. VDD = 1.8 V± 0.1V; VDDQ = 1.8 V± 0.1V.
2. IDD specifications are tested after the device is properly initialized.
3. Input slew rate is specified by AC Parametric Test Condition.
4. IDD parameters are specified with ODT disabled.
5. Data Bus consists of DQ, LDM, UDM, LDQS, /LDQS , UDQS and /UDQS .
6. Definitions for IDD

   LOW = Vin≦VIL (ac) (max)

   HIGH = Vin≧VIH (ac) (min)

   STABLE = inputs stable at a HIGH or LOW level

   FLOATING = inputs at VREF = VDDQ/2

   SWITCHING = inputs changing between HIGH and LOW every other clock cycle (once per two clocks) for address and control signals, and inputs changing between HIGH and LOW every other data transfer (once per clock) for DQ signals not including masks or strobes.

9.10. IDD Measurement Test Parameters

SPEED GRADE	DDR2-1066 (-18)	DDR2-800 (-25)	DDR2-667 (-3)	UNIT
Bin(CL-tRCD-tRP)	**7-7-7**	**6-6-6**	**5-5-5**	
CL(IDD)	7	6	5	tCK
tCK(IDD)	1.875	2.5	3	nS
tRCD(IDD)	13.125	15	15	nS
tRP(IDD)	13.125	15	15	nS
tRC(IDD)	53.125	55	55	nS
tRASmin(IDD)	40	40	40	nS
tRASmax(IDD)	70000	70000	70000	nS
tRRD(IDD)-2KB	10	10	10	nS
tFAW(IDD)-2KB	45	45	50	nS
tRFC(IDD)	127.5	127.5	127.5	nS

9.11. AC Characteristics

9.11.1. AC Characteristics and Operating Condition for -18 speed grade

SYM	SPEED GRADE		DDR2-1066 (-18)		UNIT	NOTES
	Bin(CL-tRCD-tRP)		7-7-7		tCK	
	PARAMETER		MIN	MAX	-	
tRCD	Active to Read/Write Command Delay Time		13.125	-	nS	
tRP	Precharge to Active Command Period		13.125	-		
tRC	Active to Ref/Active Command Period		53.125	-		
tRAS	Active to Precharge Command Period		40	70000		
tRFC	Auto Refresh to Active/Auto Refresh command period		127.5	-		1
tREFI	Average periodic refresh Interval	0°C ≦ TCASE ≦ 85°C	-	7.8	uS	1
		85°C ≦ TCASE ≦ 95°C	-	3.9		1,2
tCCD	Read/Write(a) to Read/Write(b) Command Period		2	-	tCK	
tCK	Clock Cycle Time	tCK @ CL=4	3.75	7.5	nS	
		tCK @ CL=5	3	7.5		
		tCK @ CL=6	1.875	7.5		
		tCK @ CL=7	1.875	7.5		
tCH	CLK, /CLK high-level width		0.48	0.52	tCK	
tCL	CLK, /CLK low-level width		0.48	0.52		
tHP	Clock half pulse width		Min.(tCH, tCL)	-		3
tAC	DQ output access time from CLK/ /CLK		-350	+350	pS	
tCKE	CKE minimum high and low pulse width		3	-	tCK	4
tRRD	Active to active command period for 2KB page size		10	-	nS	5
tFAW	Four Activate Window for 2KB page size		45			
tWR	Write recovery time		15	-		
tDAL	Auto-precharge write recovery + precharge time		WR + tRP	-	tCK	6
tWTR	Internal Write to Read command delay		7.5	-	nS	7
tRTP	Internal Read to Precharge command delay		7.5	-		8
tIS (base)	Address and control input setup time		125	-	pS	
tIH (base)	Address and control input hold time		200	-		
tIPW	Address and control input pulse width for each input		0.6	-	tCK	
tDQSS	DQS latching rising transitions to associated clock edges		-0.25	+0.25		
tDSS	DQS falling edge to CLK setup time		0.2	-		
tDSH	DQS falling edge hold time from CLK		0.2	-		
tDQSH	DQS input high pulse width		0.35	-		
tDQSL	DQS input low pulse width		0.35	-		

AC Characteristics and Operating Condition for -18 speed grade, continued

SYM	SPEED GRADE	DDR2-1066 (-18)		UNIT	NOTES
	Bin(CL-tRCD-tRP)	7-7-7		tCK	
	PARAMETER	MIN	MAX	-	
tWPRE	Write preamble	0.35	-	tCK	
tWPST	Write postamble	0.4	0.6	tCK	9
tDQSCK	DQS output access time from CLK / /CLK	-325	+325	pS	
tDQSQ	DQS-DQ skew for DQS & associated DQ signals	-	175	pS	10
tRPRE	Read preamble	0.9	1.1	tCK	11
tRPST	Read postamble	0.4	0.6	tCK	11
tDS(base)	DQ and DM input setup time	0	-	pS	
tDH(base)	DQ and DM input hold time	75	-	pS	
tDIPW	DQ and DM input pulse width for each input	0.35	-	tCK	
tHZ	Data-out high-impedance time from CLK/ /CLK	-	tAC,max	pS	11
tLZ(DQS)	DQS/ /DQS-low-impedance time from CLK/ /CLK	tAC,min	tAC,max	pS	11
tLZ(DQ)	DQ low-impedance time from CLK/ /CLK	2 x tAC,min	tAC,max	pS	11
tQHS	Data hold skew factor	-	250	pS	
tQH	DQ/DQS output hold time from DQS	tHP – tQHS	-	pS	
tXSNR	Exit Self Refresh to a non-Read command	tRFC + 10	-	nS	
tXSRD	Exit Self Refresh to a Read command	200	-	tCK	
tXP	Exit precharge power down to any command	3	-	tCK	
tXARD	Exit active power down to Read command	3	-	tCK	12
tXARDS	Exit active power down to Read command (slow exit, lower power)	10 – AL	-	tCK	12,13
tAOND	ODT turn-on delay	2	2	tCK	14
tAON	ODT turn-on	tAC,min	tAC,max + 2.575	nS	
tAONPD	ODT turn-on (Power Down mode)	tAC,min + 2	3 x tCK + tAC,max + 1	nS	
tAOFD	ODT turn-off delay	2.5	2.5	tCK	
tAOF	ODT turn-off	tAC,min	tAC,max + 0.6	nS	15
tAOFPD	ODT turn-off (Power Down mode)	tAC,min + 2	2.5 x tCK + tAC,max + 1	nS	
tANPD	ODT to power down Entry Latency	4	-	tCK	
tAXPD	ODT Power Down Exit Latency	11	-	tCK	
tMRD	Mode Register Set command cycle time	2	-	tCK	
tMOD	MRS command to ODT update delay	0	12	nS	
tOIT	OCD Drive mode output delay	0	12	nS	
tDELAY	Minimum time clocks remain ON after CKE asynchronously drops LOW	tIS + tCK + tIH	-	nS	16

9.11.2. AC Characteristics and Operating Condition for -25/-3 speed grade

SYM	SPEED GRADE		DDR2-800 (-25)		DDR2-667 (-3)		UNIT	NOTES
	Bin(CL-tRCD-tRP)		6-6-6		5-5-5		tCK	
	PARAMETER		MIN	MAX	MIN	MAX	-	
tRCD	Active to Read/Write Command Delay Time		15	-	15	-	nS	
tRP	Precharge to Active Command Period		15	-	15	-	nS	
tRC	Active to Ref/Active Command Period		55	-	55	-	nS	
tRAS	Active to Precharge Command Period		40	70000	40	70000	nS	
tRFC	Auto Refresh to Active/Auto Refresh command period		127.5	-	127.5	-	nS	1
tREFI	Average periodic refresh Interval	0°C ≦ TCASE ≦ 85°C	-	7.8	-	7.8	uS	1
		85°C ≦ TCASE ≦ 95°C	-	3.9	-	3.9	uS	1,2
tCCD	Read/Write(a) to Read/Write(b) Command Period		2	-	2	-	CK	
tCK	Clock Cycle Time	tCK @ CL=3	5	8	5	8	nS	
		tCK @ CL=4	3.75	8	3.75	8	nS	
		tCK @ CL=5	3	8	3	8	nS	
		tCK @ CL=6	2.5	8	-	-	nS	
tCH	CLK, /CLK high-level width		0.48	0.52	0.48	0.52	tCK	
tCL	CLK, /CLK low-level width		0.48	0.52	0.48	0.52	tCK	
tHP	Clock half pulse width		Min (tCH,tCL)		Min (tCH,tCL)			3
tAC	DQ output access time from CLK/ /CLK		-400	+400	-450	+450	pS	
tCKE	CKE minimum high and low pulse width		3	-	3	-	tCK	4
tRRD	Active to active command period for 2KB page size		10	-	10	-	nS	5
tFAW	Four Activate Window for 2KB page size		45	-	50	-	nS	
tWR	Write recovery time		15	-	15	-	nS	
tDAL	Auto-precharge write recovery + precharge time		WR + tRP	-	WR + tRP	-	tCK	6
tWTR	Internal Write to Read command delay		7.5	-	7.5	-	nS	7
tRTP	Internal Read to Precharge command delay		7.5	-	7.5	-	nS	8
tIS (base)	Address and control input setup time		175	-	200	-	pS	
tIH (base)	Address and control input hold time		250	-	275	-	pS	
tIPW	Address and control input pulse width for each input		0.6	-	0.6	-	tCK	
tDQSS	DQS latching rising transitions to associated clock edges		-0.25	+0.25	-0.25	+0.25	tCK	
tDSS	DQS falling edge to CLK setup time		0.2	-	0.2	-	tCK	
tDSH	DQS falling edge hold time from CLK		0.2	-	0.2	-	tCK	
tDQSH	DQS input high pulse width		0.35	-	0.35	-	tCK	
tDQSL	DQS input low pulse width		0.35	-	0.35	-	tCK	

AC Characteristics and Operating Condition for -25/-3 speed grade, continued

SYM	SPEED GRADE	DDR2-800 (-25)		DDR2-667 (-3)		UNIT	NOTES
	Bin(CL-tRCD-tRP)	6-6-6		5-5-5		tCK	
	PARAMETER	MIN	MAX	MIN	MAX	-	
tWPRE	Write preamble	0.35	-	0.35	-	tCK	
tWPST	Write postamble	0.4	0.6	0.4	0.6	tCK	9
tDQSCK	DQS output access time from CLK / /CLK	-350	+350	-400	+400	pS	
tDQSQ	DQS-DQ skew for DQS & associated DQ signals	-	200	-	240	pS	10
tRPRE	Read preamble	0.9	1.1	0.9	1.1	tCK	11
tRPST	Read postamble	0.4	0.6	0.4	0.6	tCK	11
tDS(base)	DQ and DM input setup time	50	-	100	-	pS	
tDH(base)	DQ and DM input hold time	125	-	175	-	pS	
tDIPW	DQ and DM input pulse width for each input	0.35	-	0.35	-	tCK	
tHZ	Data-out high-impedance time from CLK/ /CLK	-	tAC,max	-	tAC,max	pS	11
tLZ(DQS)	DQS/ /DQS-low-impedance time from CLK/ /CLK	tAC,min	tAC,max	tAC,min	tAC,max	pS	11
tLZ(DQ)	DQ low-impedance time from CLK/ /CLK	2 x tAC,min	tAC,max	2 x tAC,min	tAC,max	pS	11
tQHS	Data hold skew factor	-	300	-	340	pS	
tQH	DQ/DQS output hold time from DQS	tHP – tQHS	-	tHP – tQHS	-	pS	
tXSNR	Exit Self Refresh to a non-Read command	tRFC + 10	-	tRFC + 10	-	nS	
tXSRD	Exit Self Refresh to a Read command	200	-	200	-	tCK	
tXP	Exit precharge power down to any command	2	-	2	-	tCK	
tXARD	Exit active power down to Read command	2	-	2	-	tCK	12
tXARDS	Exit active power down to Read command (slow exit, lower power)	8 – AL	-	7 – AL	-	tCK	12,13
tAOND	ODT turn-on delay	2	2	2	2	tCK	14
tAON	ODT turn-on	tAC,min	tAC,max + 0.7	tAC,min	tAC,max + 0.7	nS	
tAONPD	ODT turn-on (Power Down mode)	tAC,min + 2	2 x tCK + tAC,max + 1	tAC,min + 2	2 x tCK + tAC,max + 1	nS	
tAOFD	ODT turn-off delay	2.5	2.5	2.5	2.5	tCK	
tAOF	ODT turn-off	tAC,min	tAC,max + 0.6	tAC,min	tAC,max + 0.6	nS	15
tAOFPD	ODT turn-off (Power Down mode)	tAC,min + 2	2.5 x tCK + tAC,max + 1	tAC,min + 2	2.5 x tCK + tAC,max + 1	nS	
tANPD	ODT to power down Entry Latency	3	-	3	-	tCK	
tAXPD	ODT Power Down Exit Latency	8	-	8	-	tCK	
tMRD	Mode Register Set command cycle time	2	-	2	-	tCK	
tMOD	MRS command to ODT update delay	0	12	0	12	nS	
tOIT	OCD Drive mode output delay	0	12	0	12	nS	
tDELAY	Minimum time clocks remain ON after CKE asynchronously drops LOW	tIS+tCK+tIH	-	tIS+tCK+tIH	-	nS	16

Note:

1. If refresh timing is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.
2. This is an optional feature. For detailed information, please refer to “operating temperature condition” chapter 9.2 in this data sheet.
3. Min. (tCL, tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device.
4. tCKE min of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of tIS + 2 x tCK + tIH.
5. A minimum of two clocks (2 * tCK) is required irrespective of operating frequency.
6. tDAL = WR + RU{ tRP[nS] / tCK[nS] }, where RU stands for round up. WR refers to the tWR parameter stored in the MRS. For tRP, if the result of the division is not already an integer, round up to the next highest integer. tCK refers to the application clock period.
   Example: For DDR2-533 at tCK = 3.75nS with WR programmed to 4 clocks.
   tDAL = 4 + (15 nS / 3.75 nS) clocks = 4 + (4) clocks = 8 clocks.
7. tWTR is at least two clocks (2 * tCK) independent of operation frequency.
8. This is a minimum requirement. Minimum read to precharge timing is AL + BL/2 providing that the tRTP and tRAS(min) have been satisfied.
9. The maximum limit for the tWPST parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) will degrades accordingly.
10. tDQSQ: Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output Slew Rate mismatch between DQS /DQS and associated DQ in any given cycle.
11. The tHZ, tRPST and tLZ, tRPRE parameters are referenced to a specific voltage level, which specify when the device output is no longer driving (tHZ, tPRST), or begins driving (tLZ, tRPRE). tHZ and tLZ transitions occur in the same access time windows as valid data transitions. These parameters are verified by design and characterization, but not subject to production test.
12. User can choose which active power down exit timing to use via MRS (bit 12). tXARD is expected to be used for fast active power down exit timing. tXARDS is expected to be used for slow active power down exit timing.
13. AL = Additive Latency.
14. ODT turn on time min. is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max. is when the ODT resistance is fully on. Both are measure from tAOND.
15. ODT turn off time min. is when the device starts to turn off ODT resistance. ODT turn off time max. is when the bus is in high impedance. Both are measured from tAOFD.
16. The clock frequency is allowed to change during Self Refresh mode or precharge power-down mode. In case of clock frequency change during precharge power-down, a specific procedure is required as described in Chapter 7.10.
17. Tests for AC timing, IDD, and electrical AC and DC characteristics may be conducted at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified. ODT is disabled for all measurements that are not ODT-specific.

9.12. AC Input Test Conditions

(0℃ ≦ TCASE ≦ 85℃ for -18/-25/-3, VDD, VDDQ = 1.8V ± 0.1V)

CONDITION	SYMBOL	VALUE	UNIT	NOTES
Input reference voltage	VREF	0.5 x VDDQ	V	1
Input signal maximum peak to peak swing	VSWING(MAX)	1.0	V	1
Input signal minimum slew rate	SLEW	1.0	V / nS	2,3

Note:

1. Input waveform timing is referenced to the input signal crossing through the VIH/IL(ac) level applied to the device under test.
2. The input signal minimum slew rate is to be maintained over the range from VREF to VIH(ac) min for rising edges and the range from VREF to VIL(ac) max for falling edges as shown in the below figure.
3. AC timings are referenced with input waveforms switching from VIL(ac) to VIH(ac) on the positive transitions and VIH(ac) to VIL(ac) on the negative transitions.

9.13. Differential Input AC Logic Level

(0℃ ≦ TCASE ≦ 85℃ for -18/-25/-3, VDD, VDDQ = 1.8V ± 0.1V)

PARAMETER	SYM	MIN	MAX	UNIT	NOTES
AC differential input voltage	VID(ac)	0.5	VDDQ + 0.6	V	1
AC differential cross point voltage	VIX(ac)	0.5 x VDDQ - 0.175	0.5 x VDDQ + 0.175	V	2

Note:

1. VID (ac) specifies the input differential voltage |VTR -VCP | required for switching, where VTR is the true input signal (such as CLK, LDQS or UDQS) and VCP is the complementary input signal (such as /CLK ,/ LDQS or /UDQS). The minimum value is equal to VIH (ac) - VIL (ac).
2. The typical value of VIX (ac) is expected to be about 0.5 x VDDQ of the transmitting device and VIX (ac) is expected to track variations in VDDQ. VIX (ac) indicates the voltage at which differential input signals must cross.

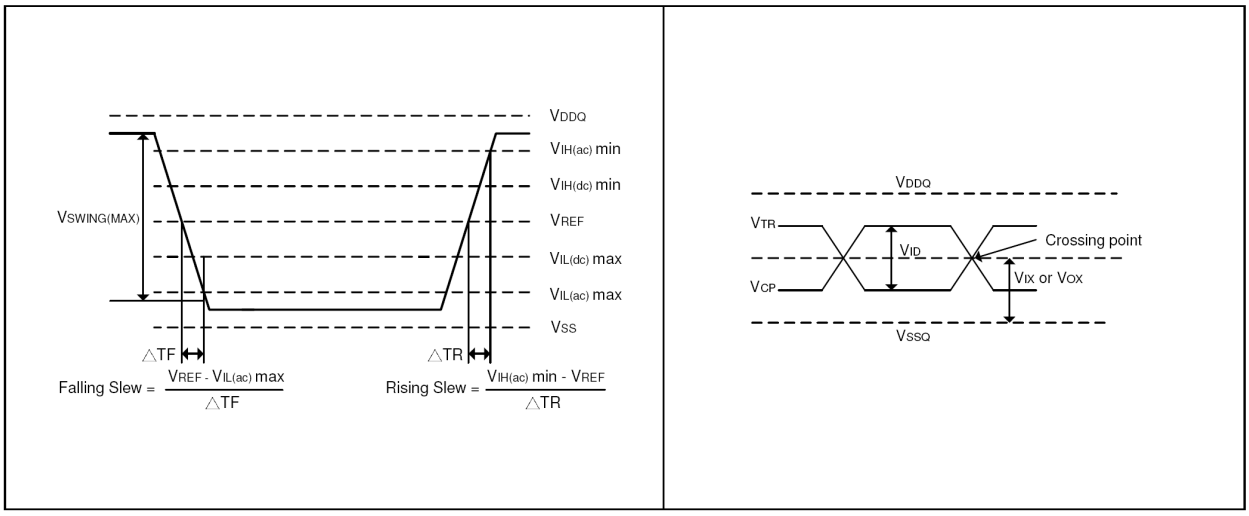


Figure 16 - AC input test signal and Differential input AC signal levels waveform

9.14. Differential AC Output Parameter

(0℃ ≦ TCASE ≦ 85℃ for -18/-25/-3, VDD, VDDQ = 1.8V ± 0.1V)

PARAMETER	SYM	MIN	MAX	UNIT	NOTES
AC differential cross point voltage	VOX(ac)	0.5 x VDDQ - 0.125	0.5 x VDDQ + 0.125	V	1

Note:

1. The typical value of VOX (ac) is expected to be about 0.5 x VDDQ of the transmitting device and VOX (ac) is expected to track variations in VDDQ. VOX (ac) indicates the voltage at which differential output signals must cross.

9.15. AC Overshoot / Undershoot Specification

9.15.1. AC Overshoot / Undershoot Specification for Address and Control Pins:

Applies to A0-A12, BA0-BA1, /CS, /RAS, /CAS, /WE, CKE, ODT

PARAMETER	-18	-25	-3	UNIT
Maximum peak amplitude allowed for overshoot area	0.9	0.9	0.9	V
Maximum peak amplitude allowed for undershoot area	0.9	0.9	0.9	V
Maximum overshoot area above VDD	0.5	0.66	0.8	V-nS
Maximum undershoot area below VSS	0.5	0.66	0.8	V-nS

9.15.2. AC Overshoot / Undershoot Specification for Clock, Data, Strobe and Mask pin:

Applies to DQ, LDQS, /LDQS, UDQS, /UDQS, LDM, UDM, CLK, /CLK

PARAMETER	-18	-25	-3	UNIT
Maximum peak amplitude allowed for overshoot area	0.9	0.9	0.9	V
Maximum peak amplitude allowed for undershoot area	0.9	0.9	0.9	V
Maximum overshoot area above VDD	0.19	0.23	0.23	V-nS
Maximum undershoot area below VSS	0.19	0.23	0.23	V-nS

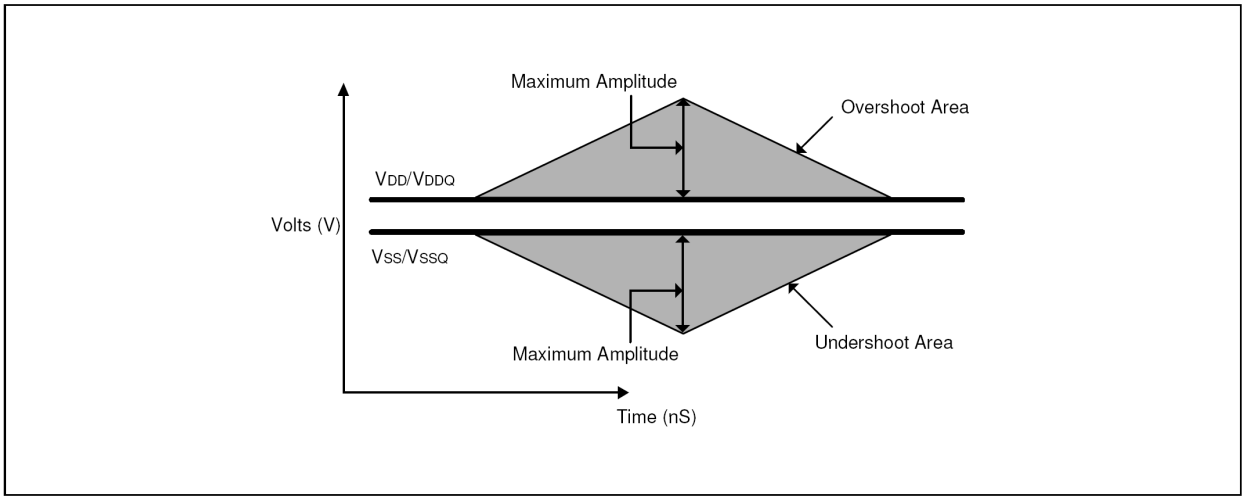
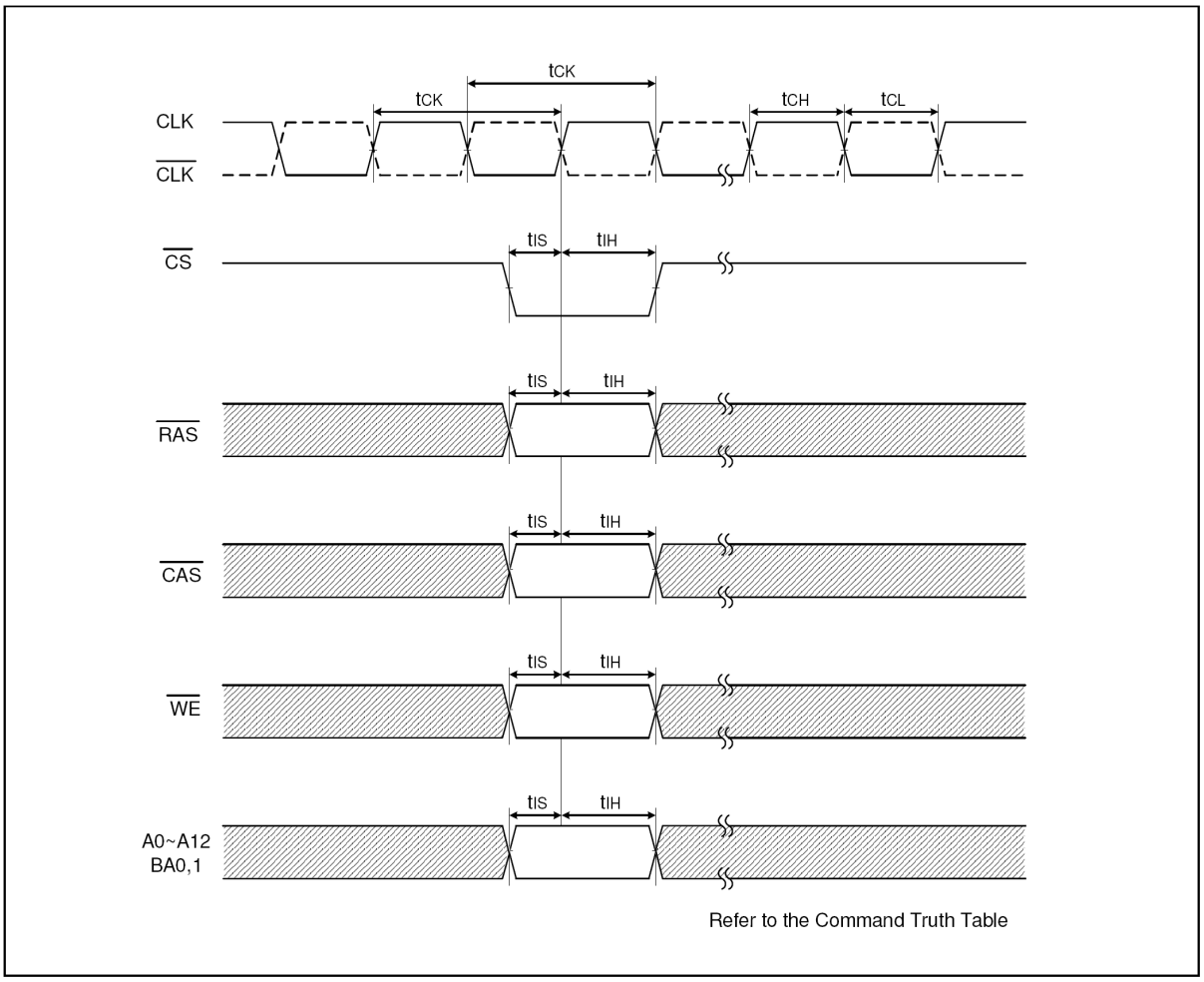


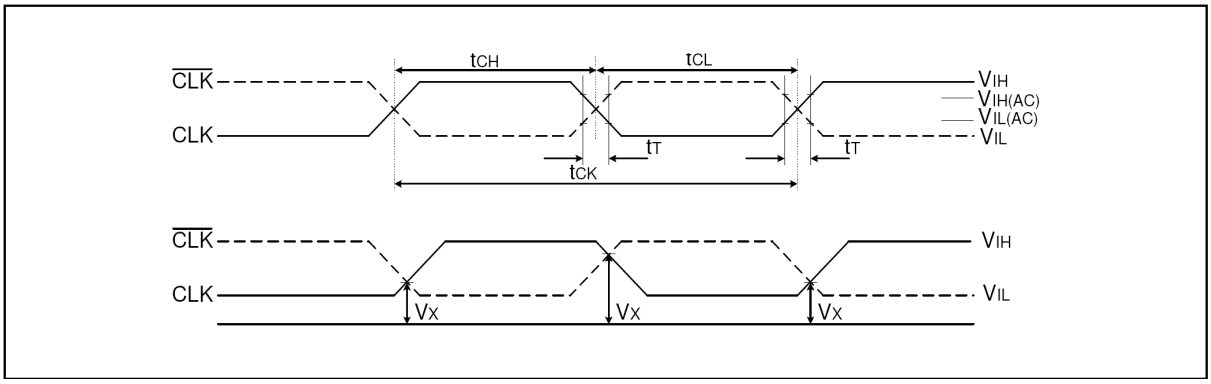
Figure 17 - AC overshoot and undershoot definition

10. TIMING WAVEFORMS

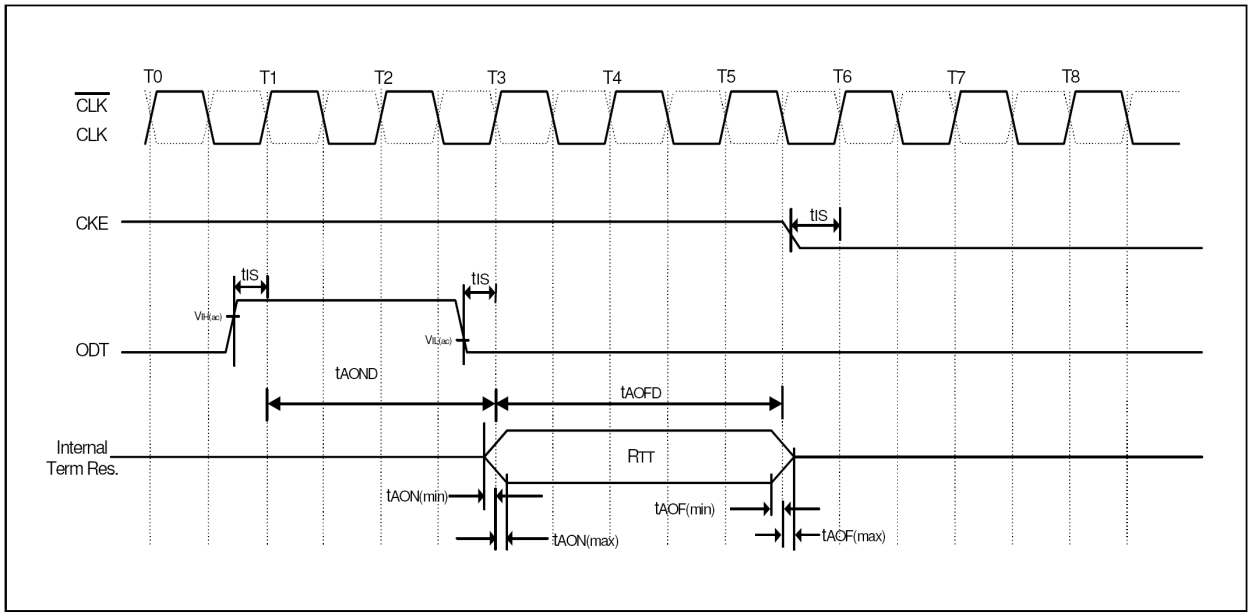
10.1. Command Input Timing



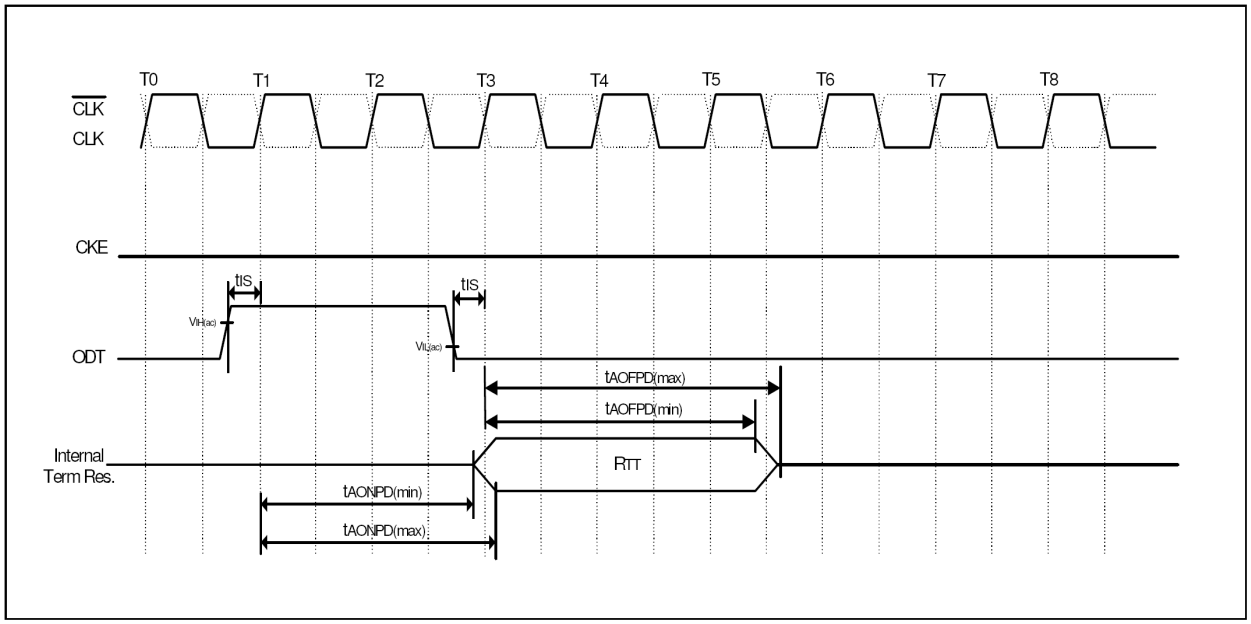
10.2. Timing of the CLK Signals



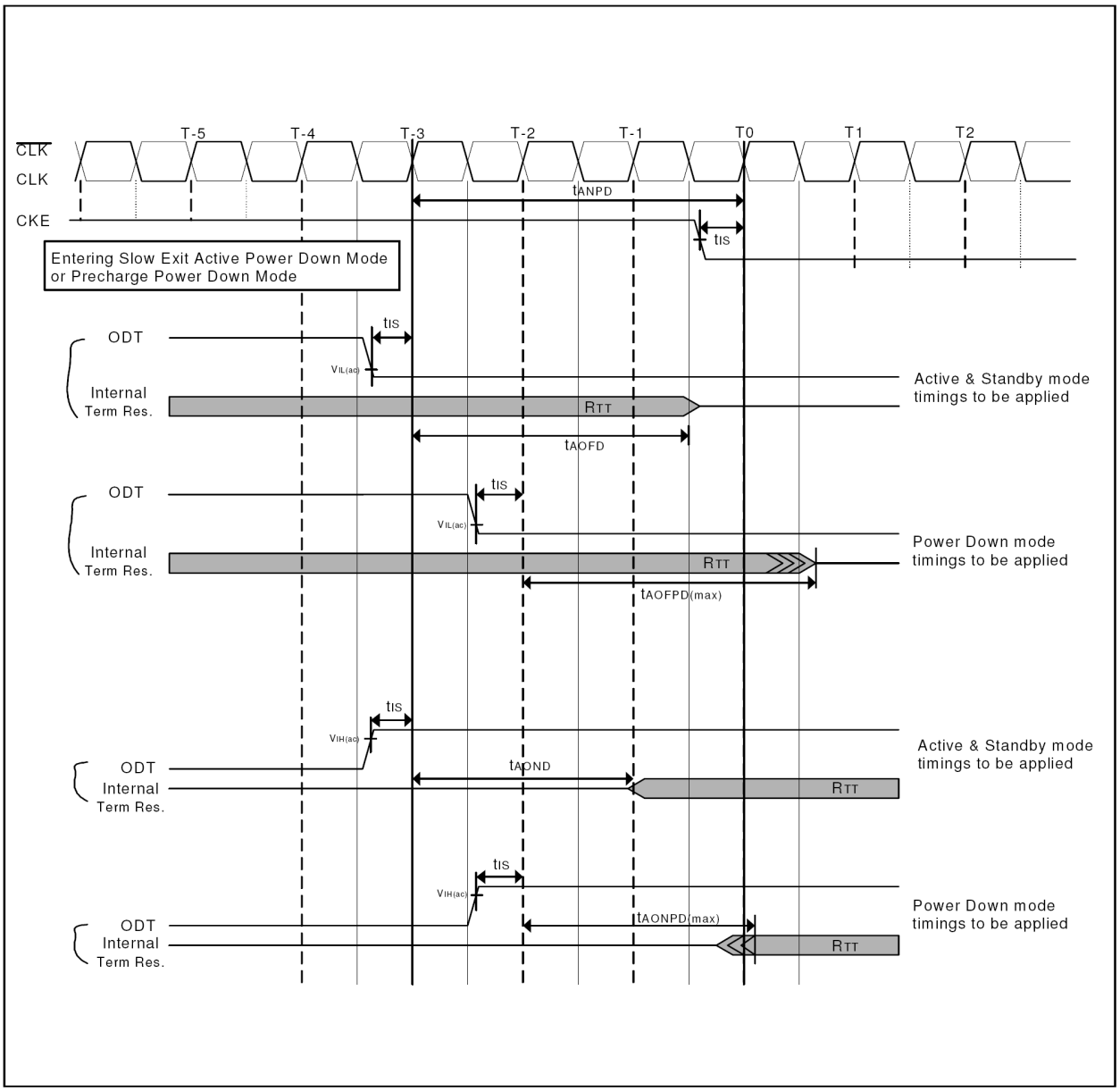
10.3. ODT Timing for Active/Standby Mode



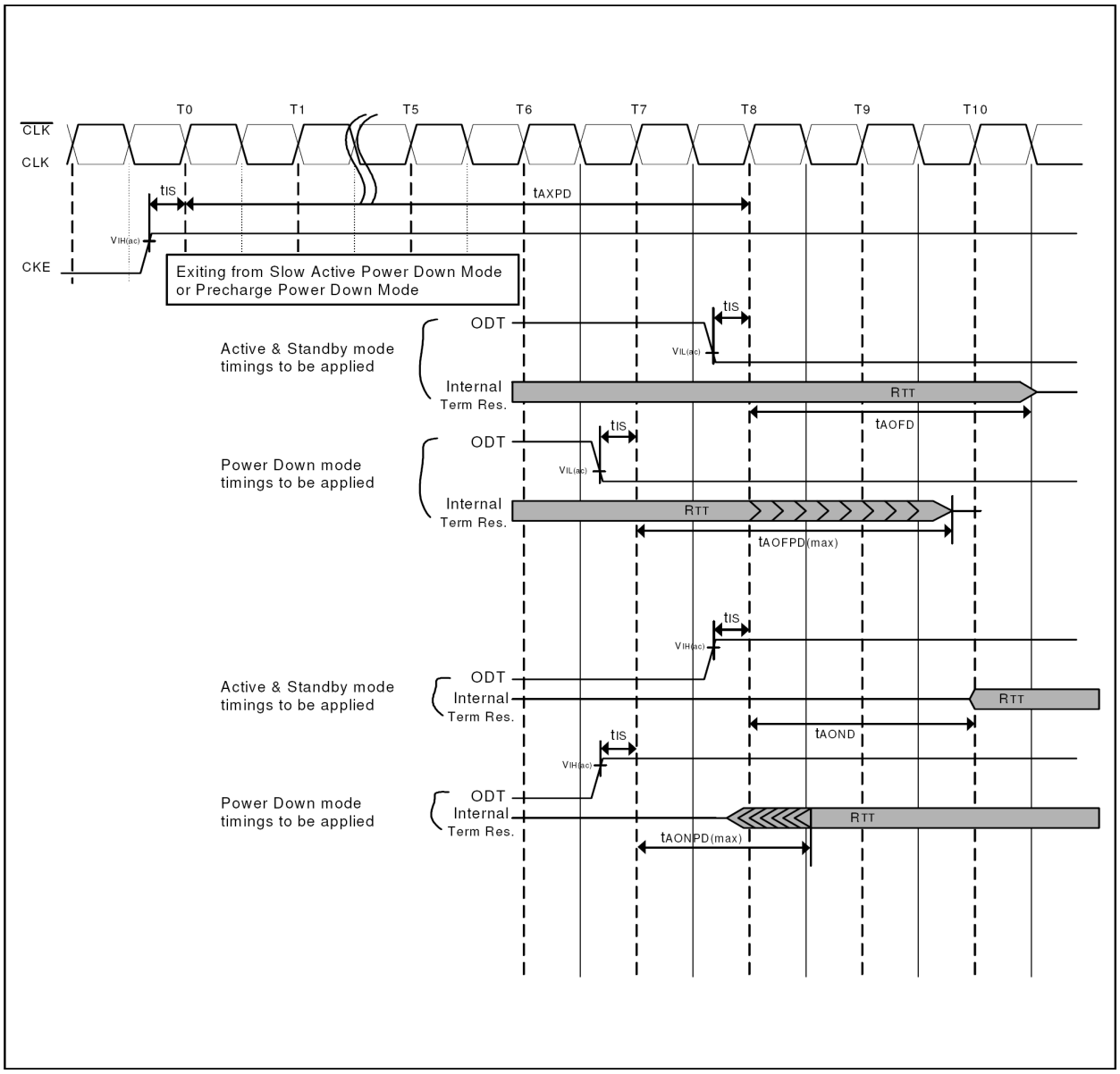
10.4. ODT Timing for Power Down Mode



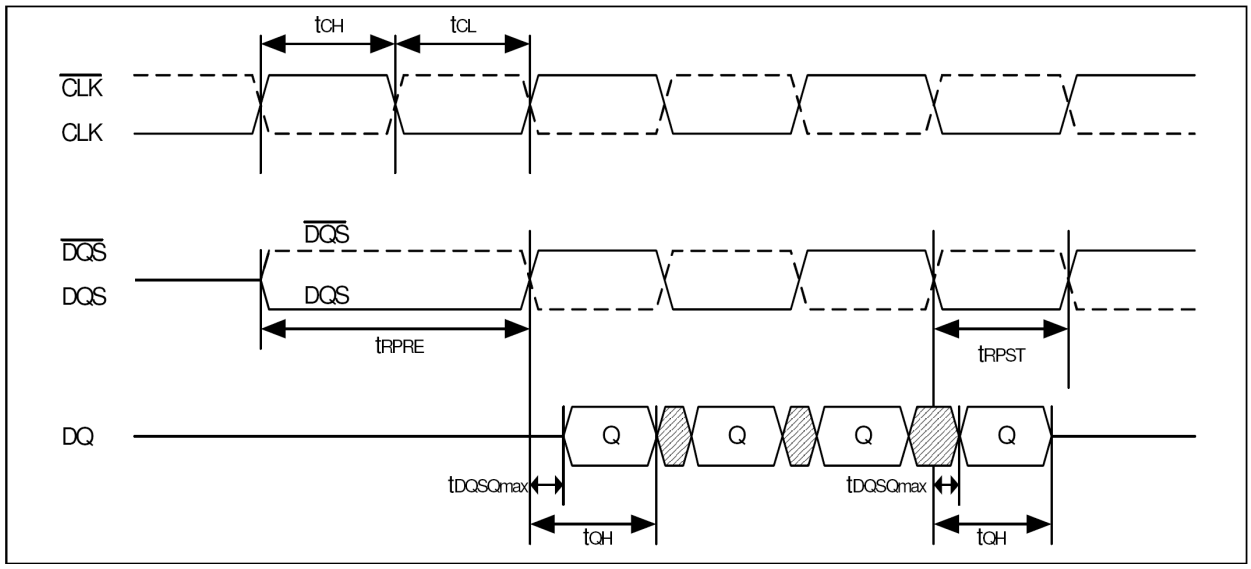
10.5. ODT Timing mode switch at entering power down mode



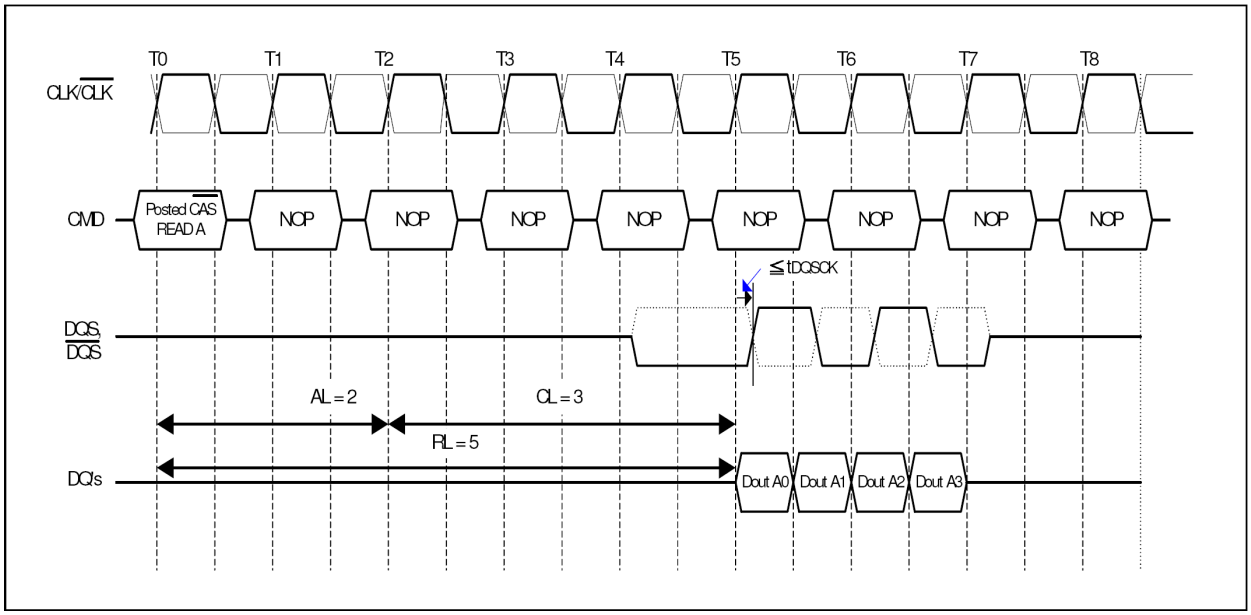
10.6. ODT Timing mode switch at exiting power down mode



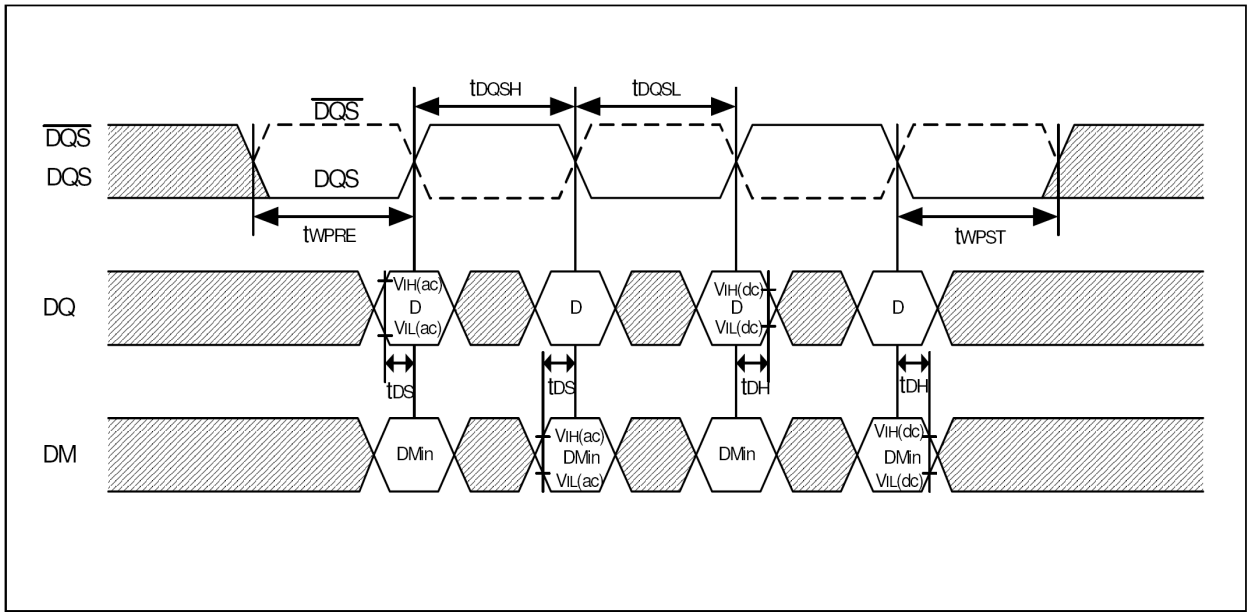
10.7. Data output (read) timing



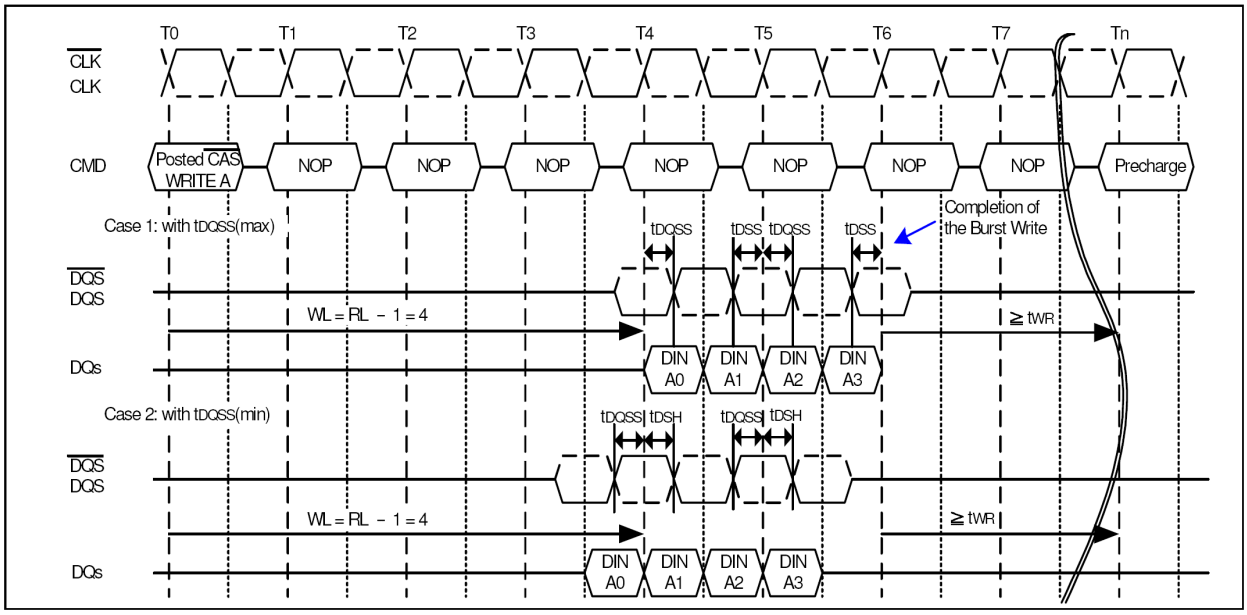
10.8. Burst read operation: RL=5 (AL=2, CL=3, BL=4)



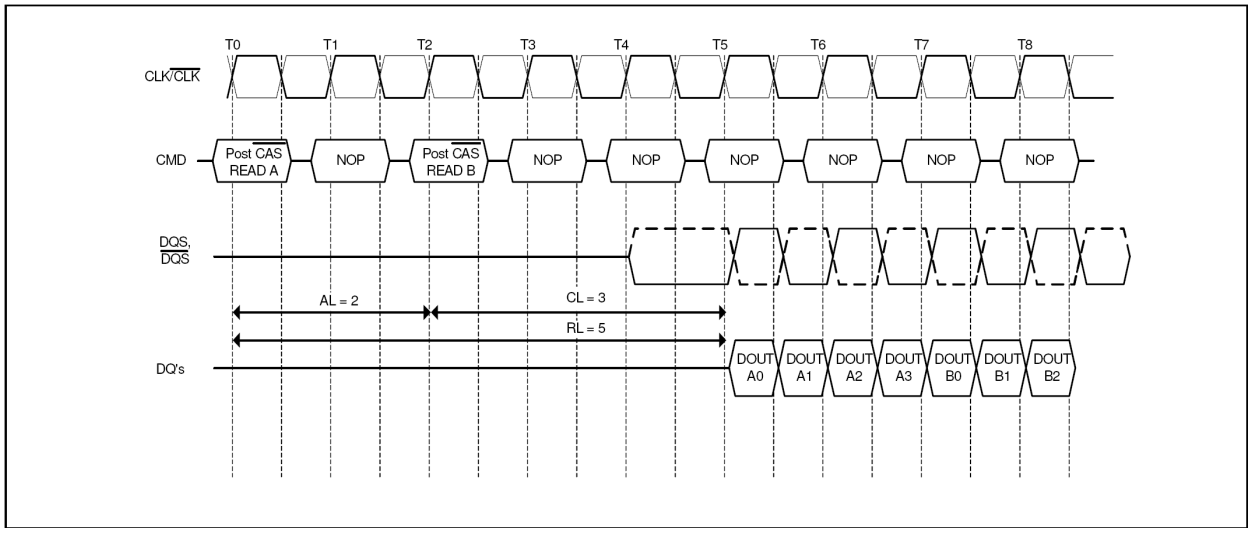
10.9. Data input (write) timing



10.10. Burst write operation: RL=5 (AL=2, CL=3, WL=4, BL=4)



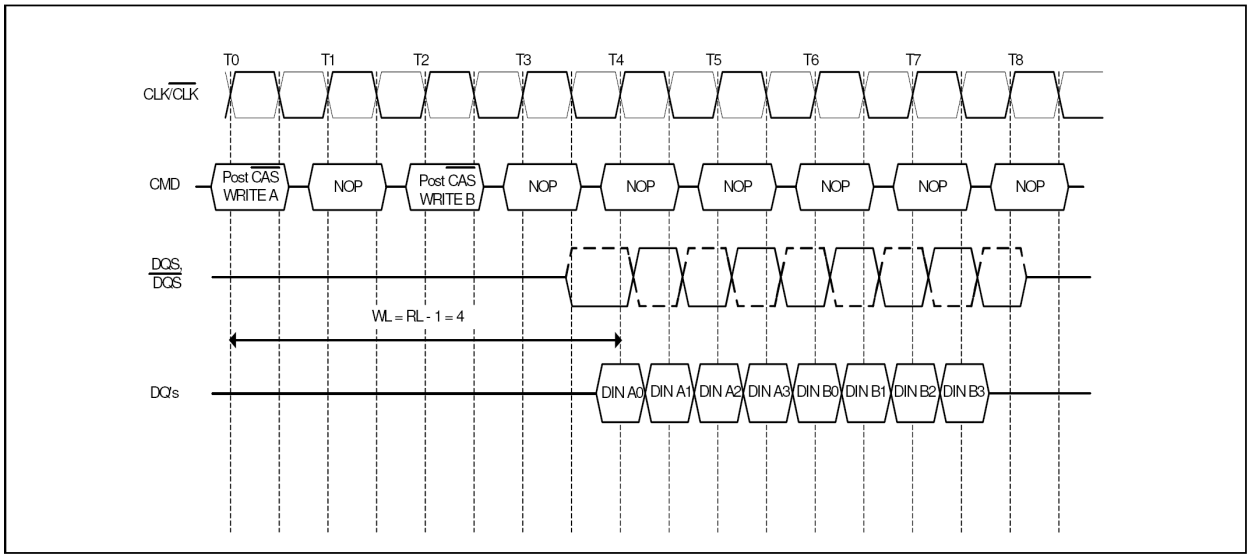
10.11. Seamless burst read operation: RL = 5 (AL = 2, and CL = 3, BL = 4)



Note:

The seamless burst read operation is supported by enabling a read command at every other clock for BL = 4 operation, and every 4 clock for BL = 8 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

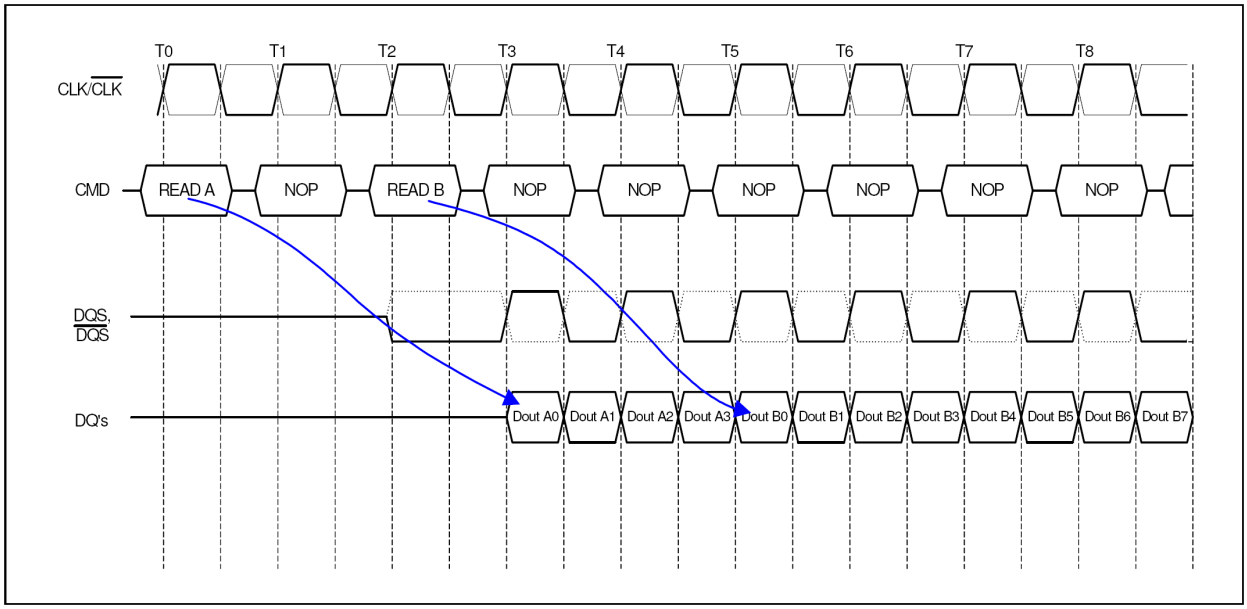
10.12. Seamless burst write operation: RL = 5 (WL = 4, BL = 4)



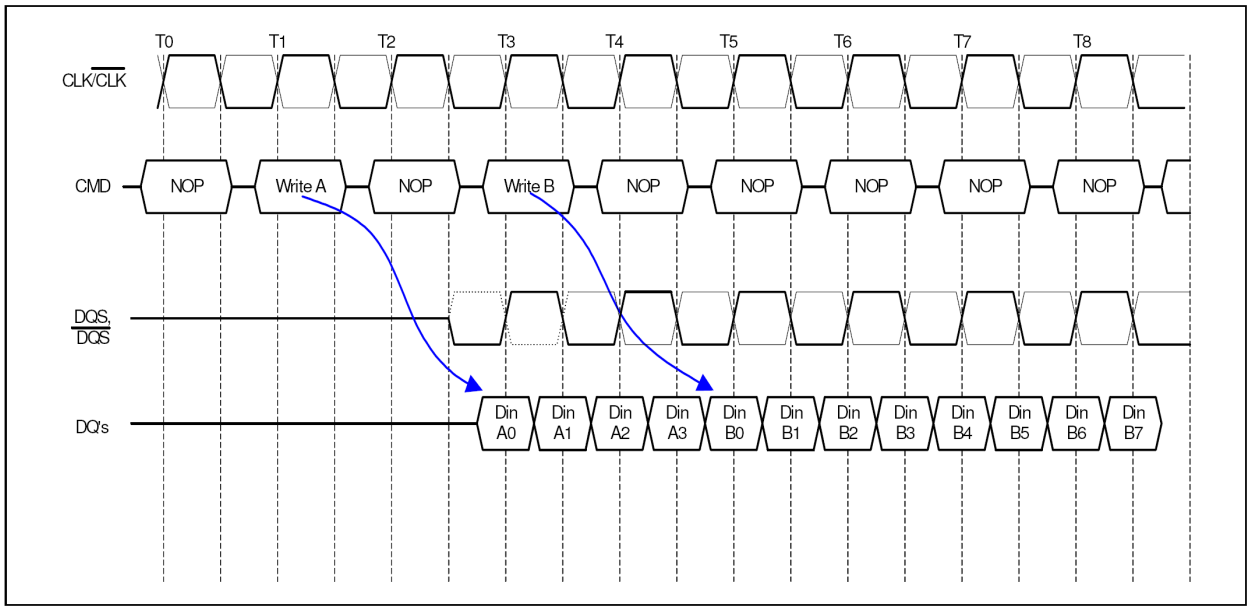
Note:

The seamless burst write operation is supported by enabling a write command every other clock for BL = 4 operation, every four clocks for BL = 8 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

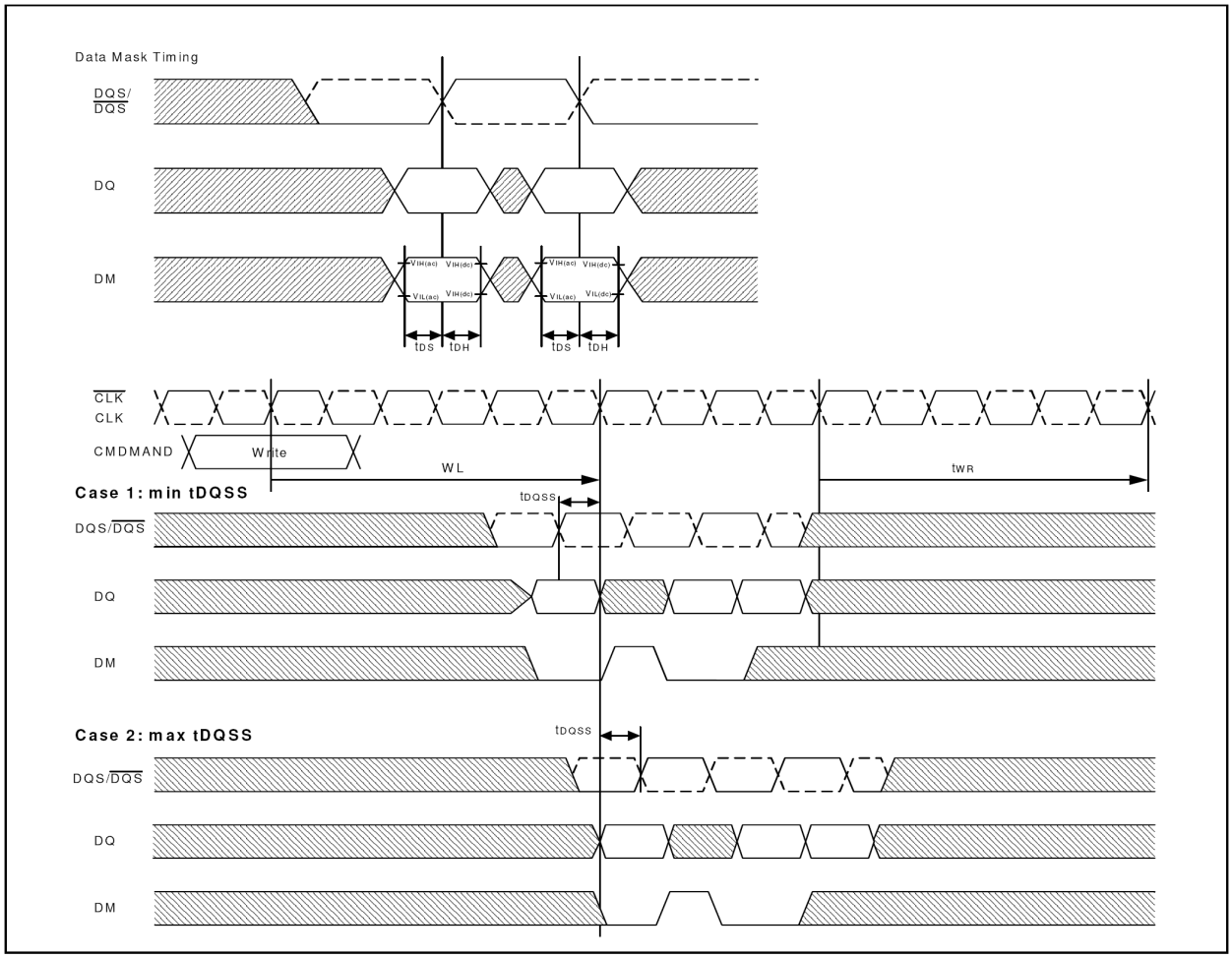
10.13. Burst read interrupt timing: RL =3 (CL=3, AL=0, BL=8)



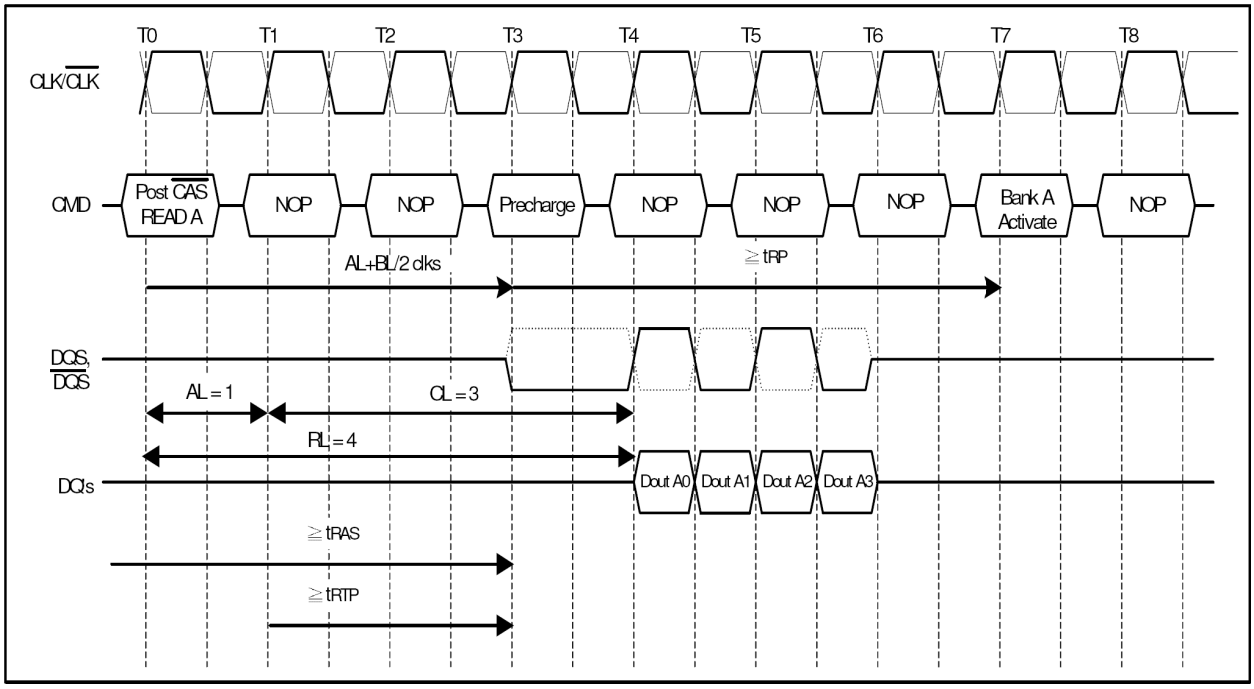
10.14. Burst write interrupt timing: RL=3 (CL=3, AL=0, WL=2, BL=8)



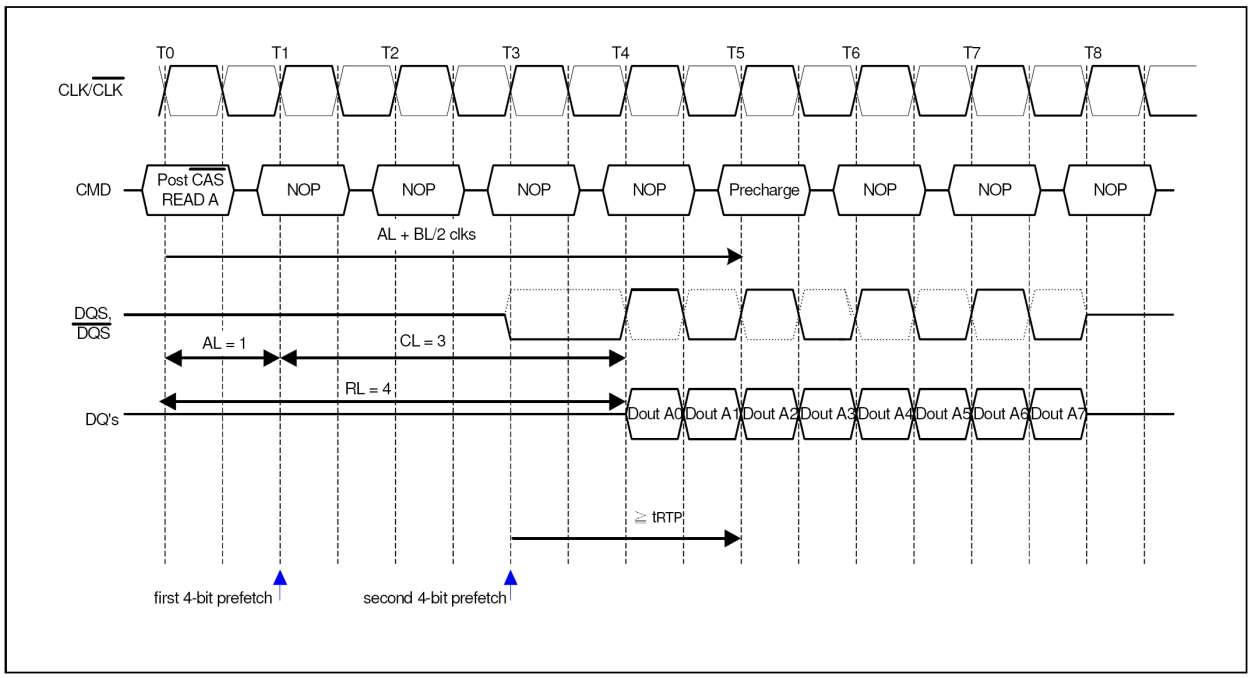
10.15.Write operation with Data Mask: WL=3, AL=0, BL=4)



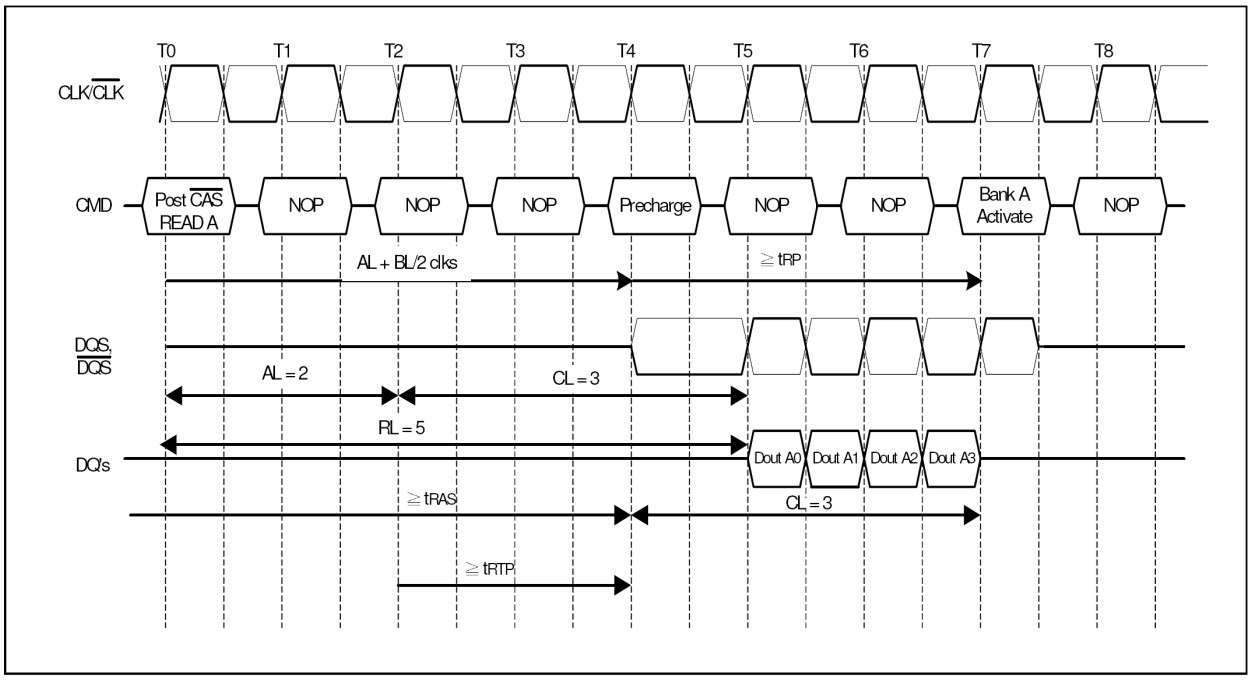
10.16. Burst read operation followed by precharge: RL=4 (AL=1, CL=3, BL=4, tRTP≦2clks)



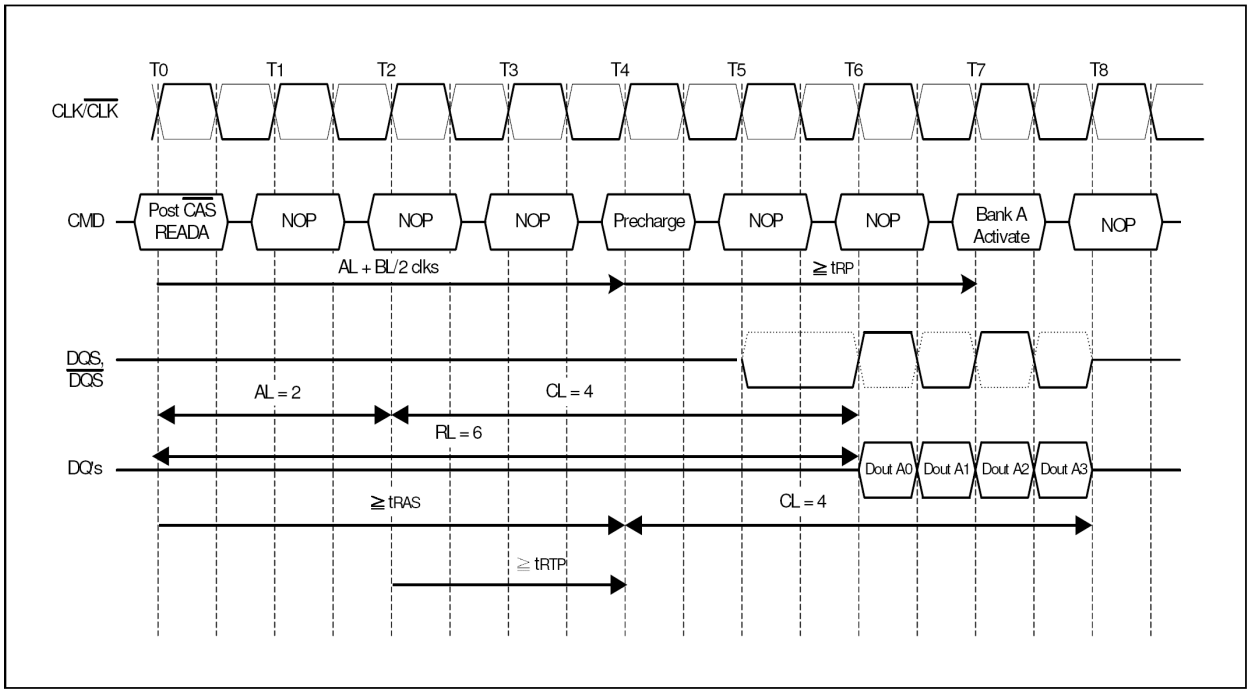
10.17. Burst read operation followed by precharge: RL=4 (AL=1, CL=3, BL=8, tRTP≦2clks)



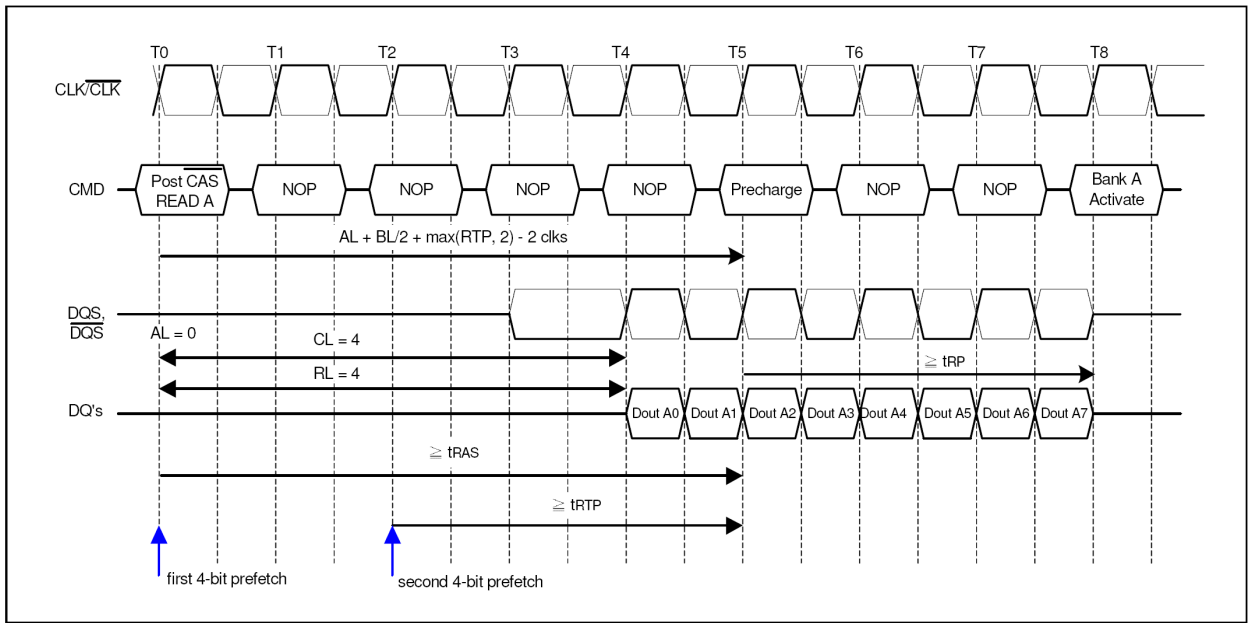
10.18. Burst read operation followed by precharge: RL=5 (AL=2, CL=3, BL=4, tRTP≦2clks)



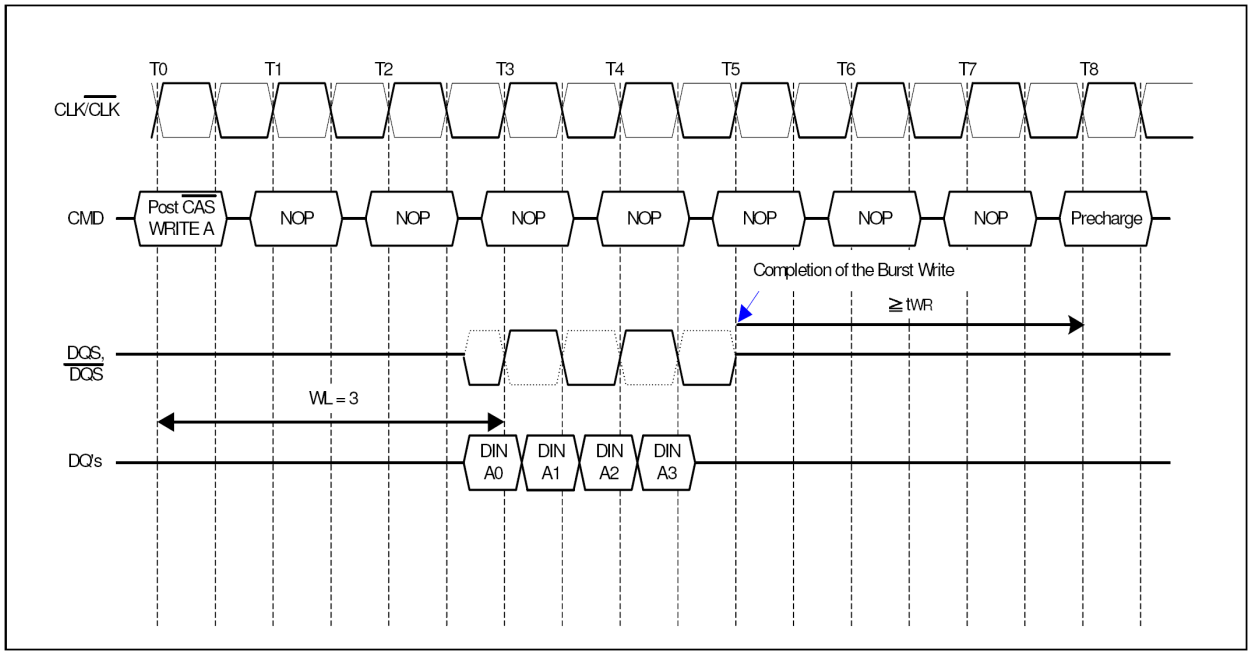
10.19. Burst read operation followed by precharge: RL=6 (AL=2, CL=4, BL=4, tRTP≦2clks)



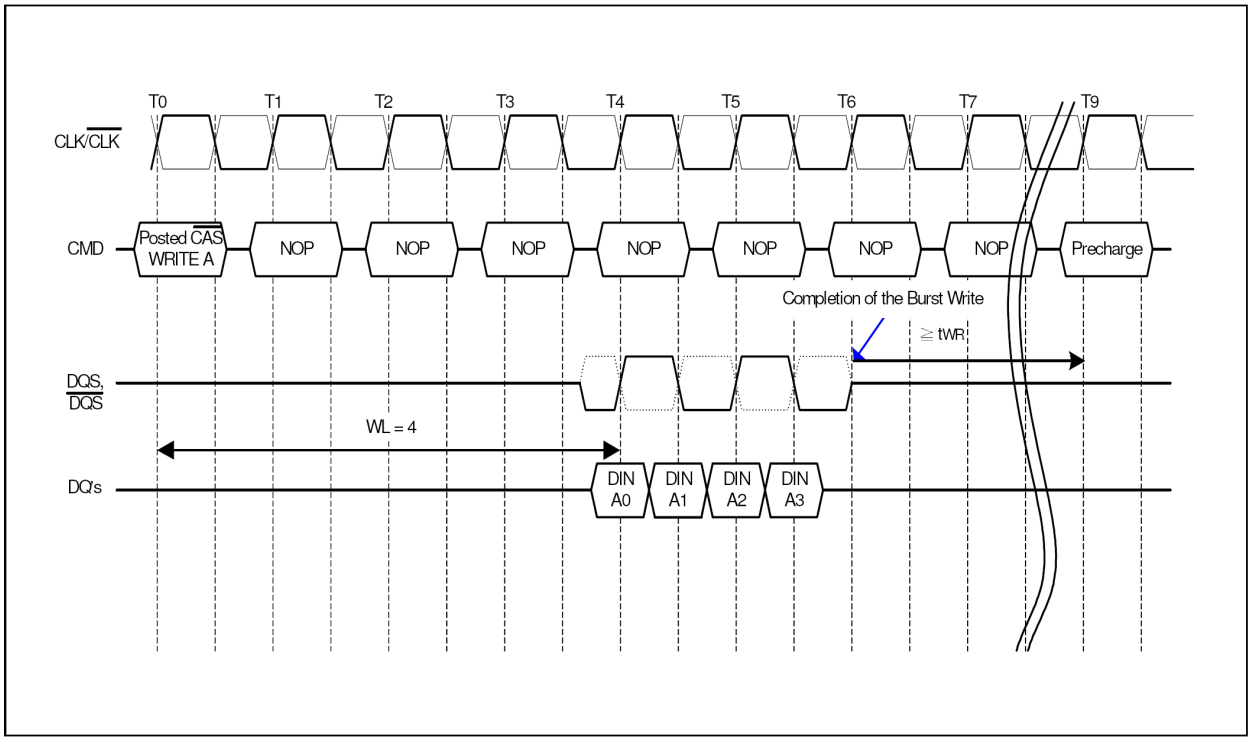
10.20. Burst read operation followed by precharge: RL=4 (AL=0, CL=4, BL=8, tRTP>2clks)



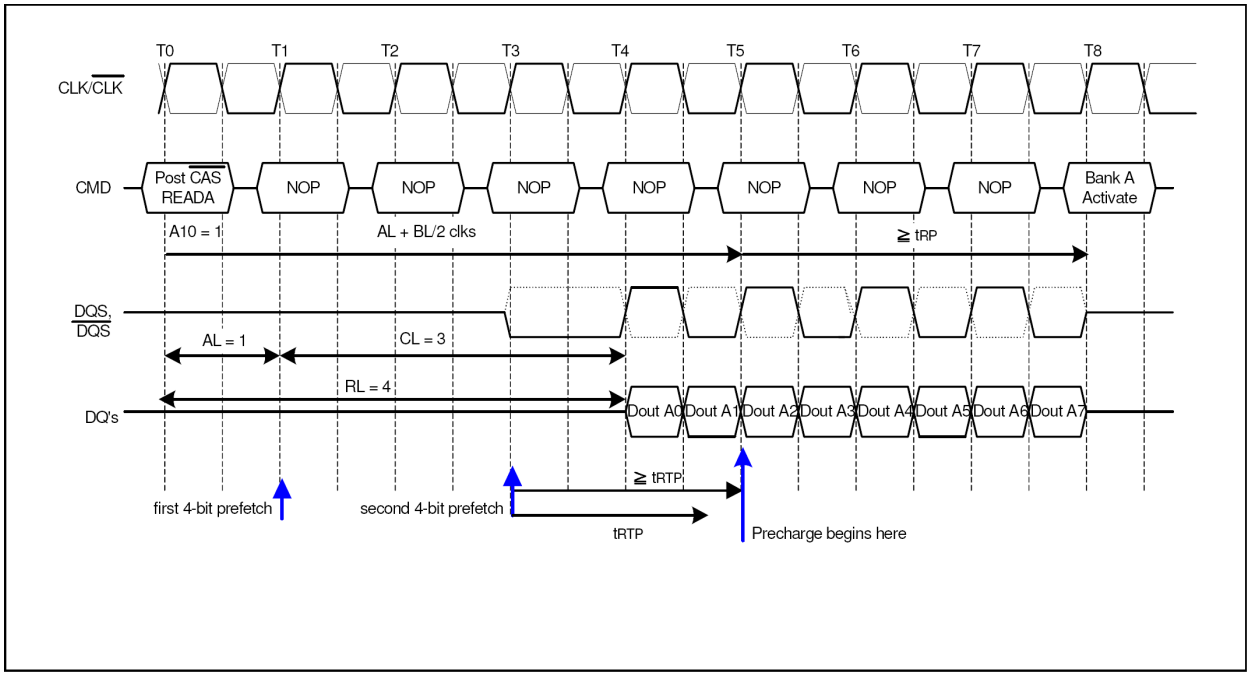
10.21. Burst write operation followed by precharge: WL = (RL-1) = 3



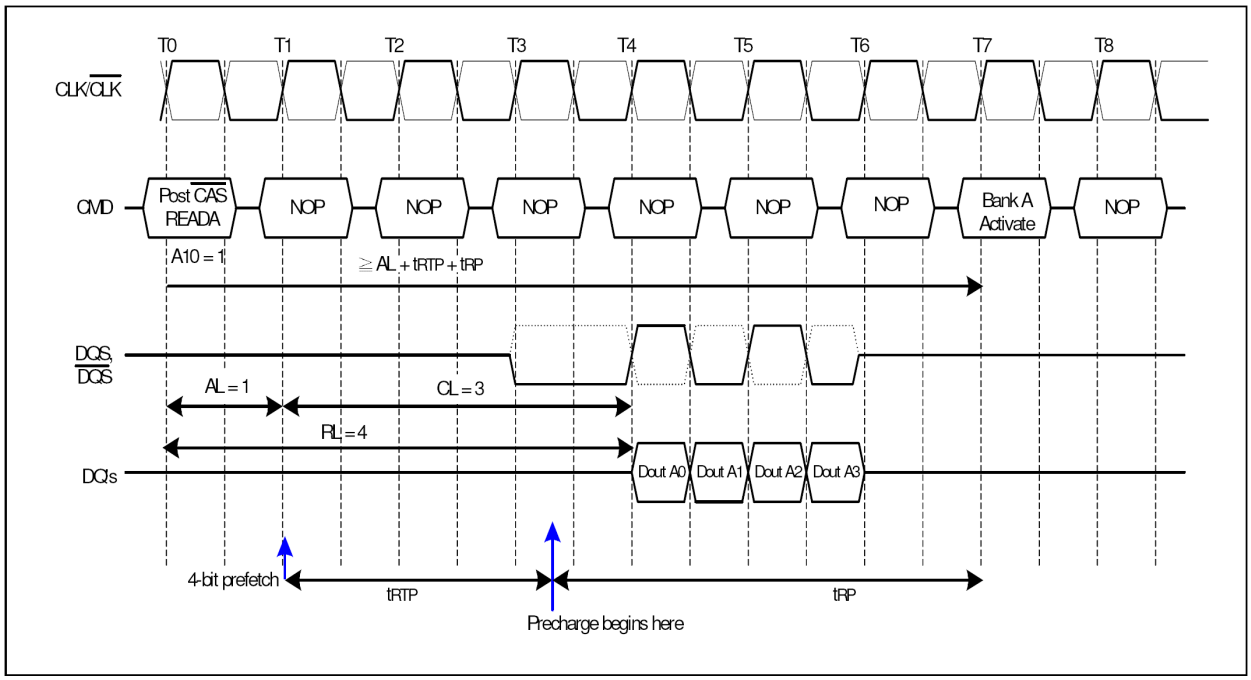
10.22. Burst write operation followed by precharge: WL = (RL-1) = 4



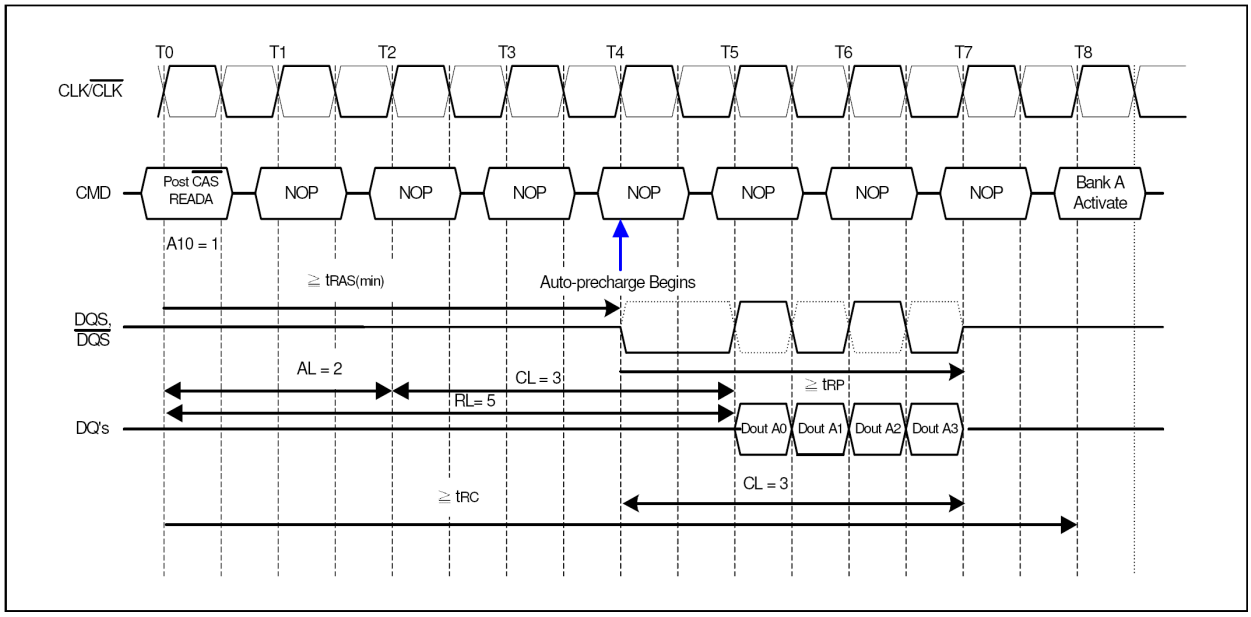
10.23. Burst read operation with Auto-precharge: RL=4 (AL=1, CL=3, BL=8, tRTP≦2clks)



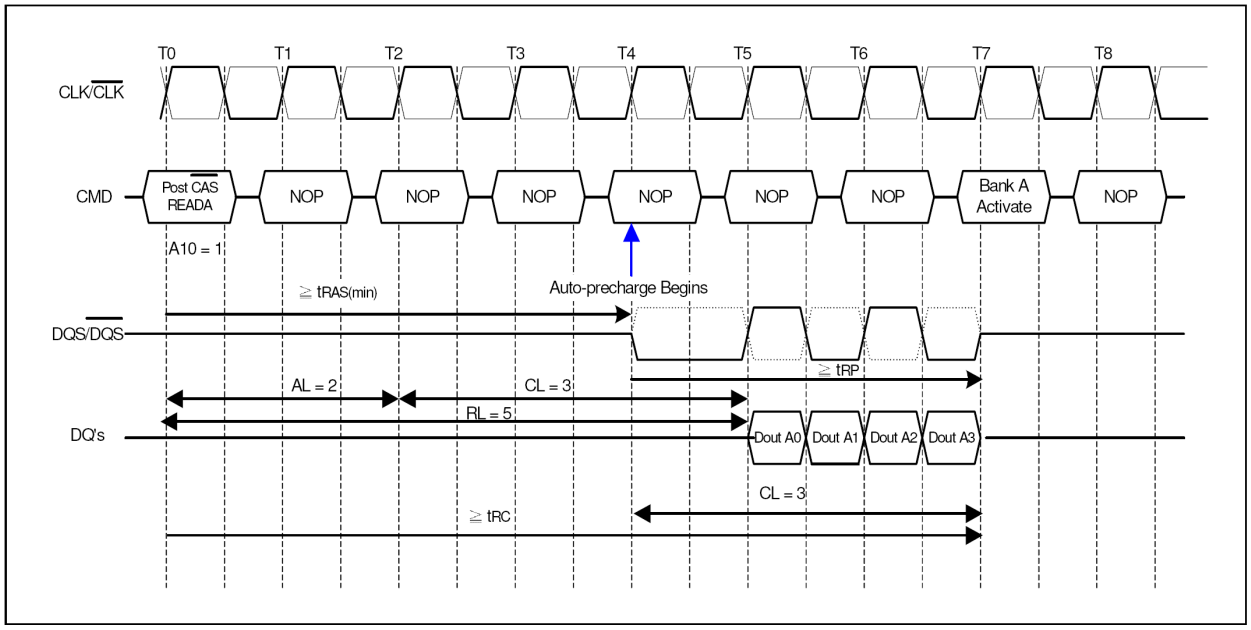
10.24. Burst read operation with Auto-precharge: RL=4 (AL=1, CL=3, BL=4, tRTP>2clks)



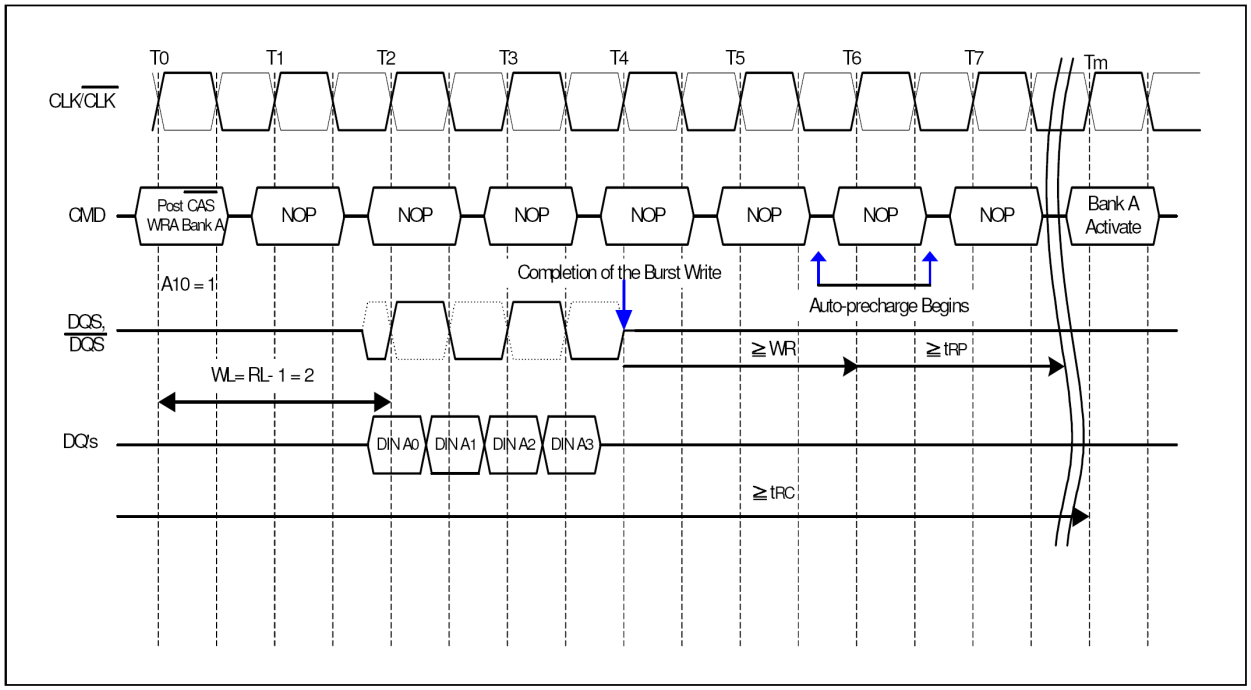
10.25. Burst read with Auto-precharge followed by an activation to the same bank (tRC Limit): RL=5 (AL=2, CL=3, internal tRCD=3, BL=4, tRTP≦2clks)



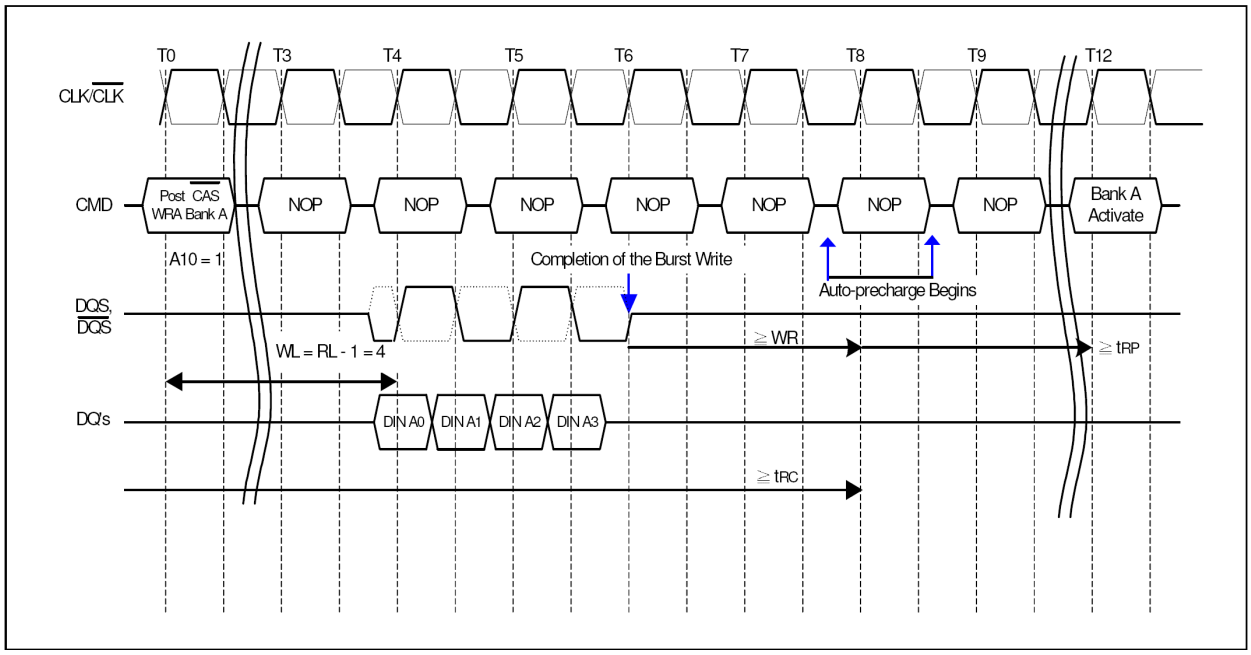
10.26. Burst read with Auto-precharge followed by an activation to the same bank (tRP Limit): RL=5 (AL=2, CL=3, internal tRCD=3, BL=4, tRTP≦2clks)



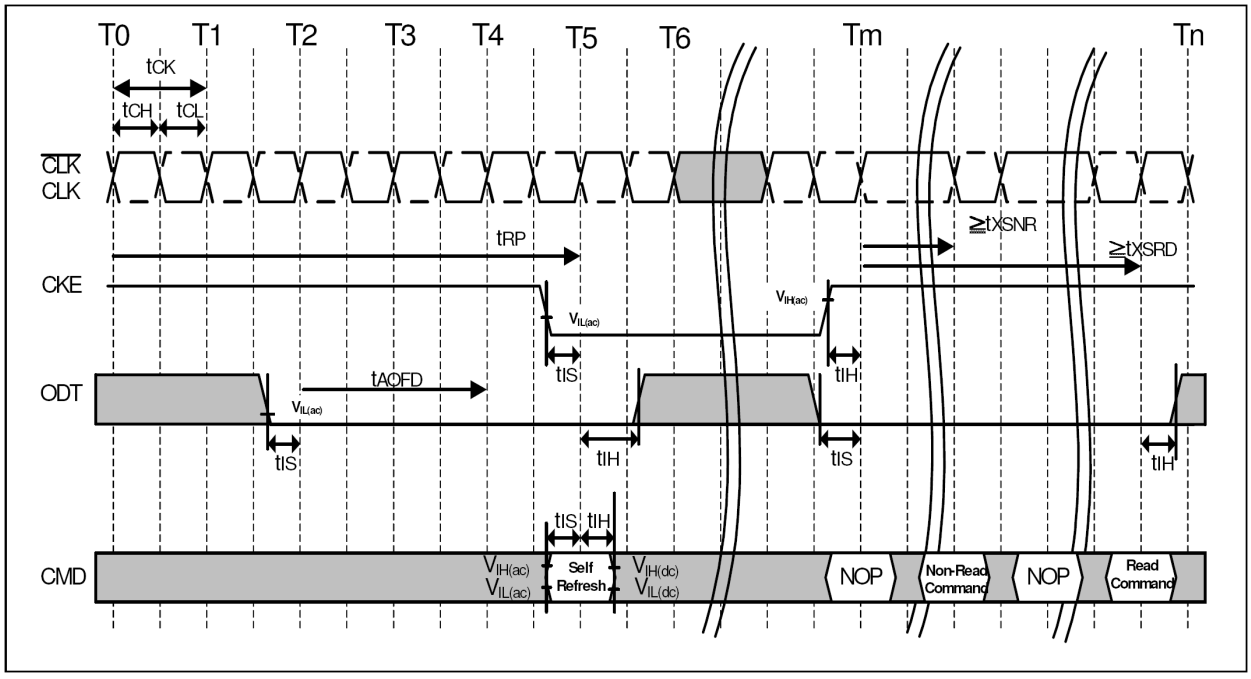
10.27. Burst write with Auto-precharge (tRC Limit): WL=2, WR=2, BL=4, tRP=3



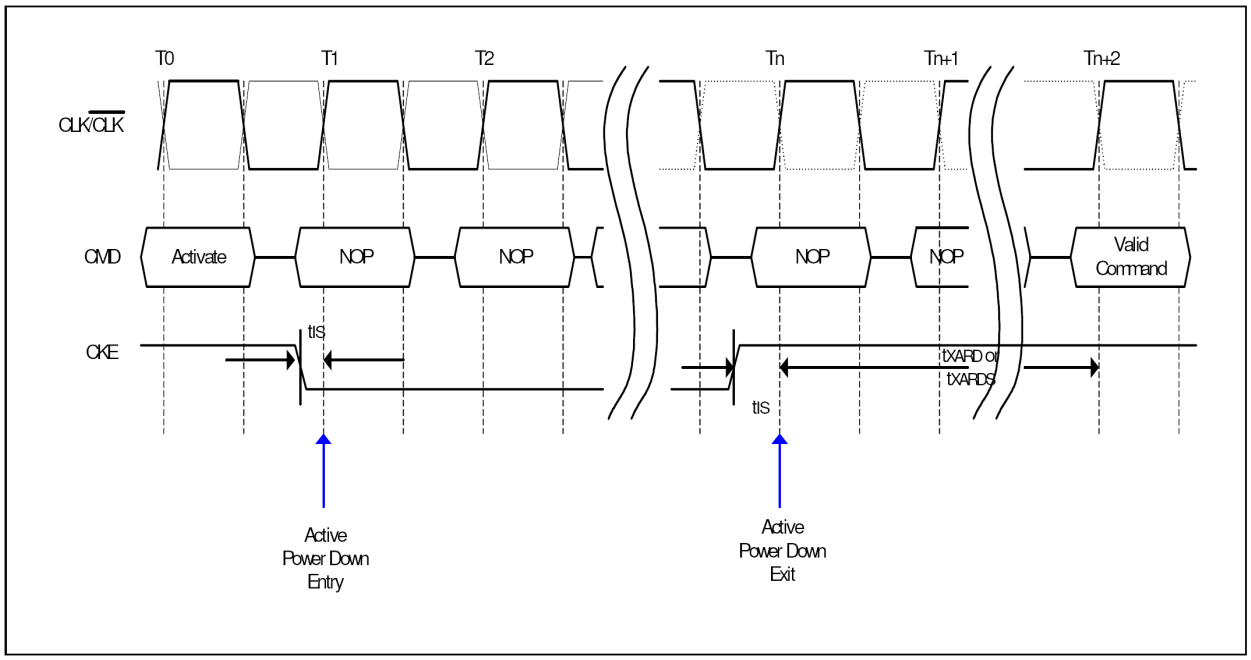
10.28. Burst write with Auto-precharge (WR + tRP): WL=4, WR=2, BL=4, tRP=3



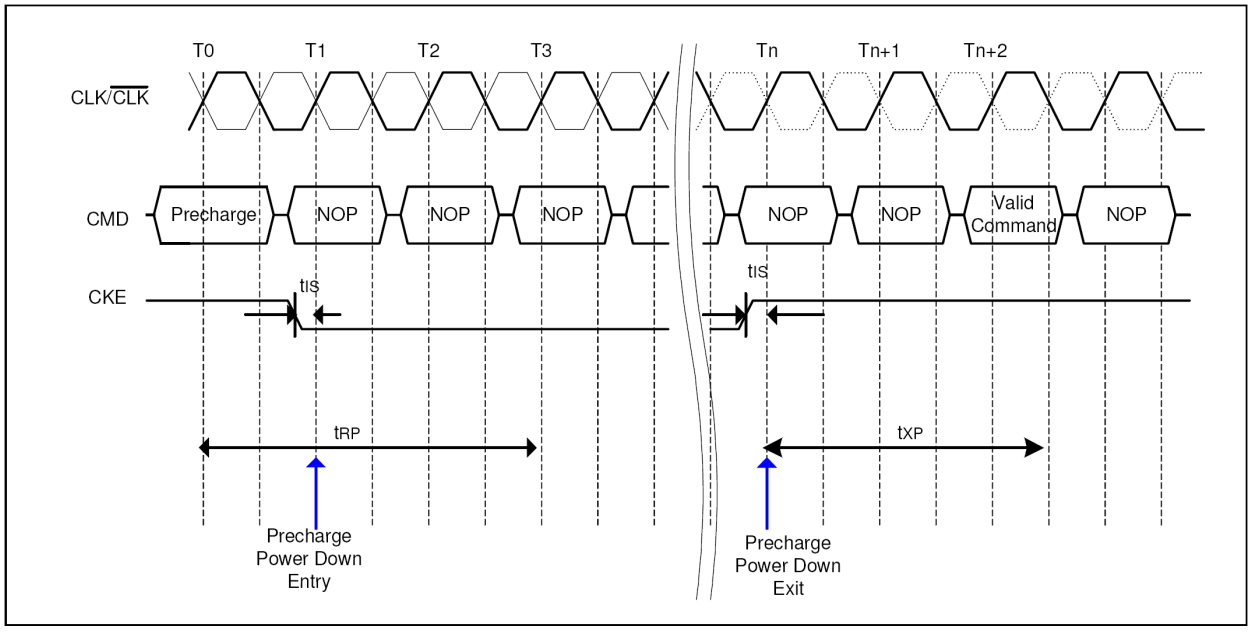
10.29. Self Refresh Timing



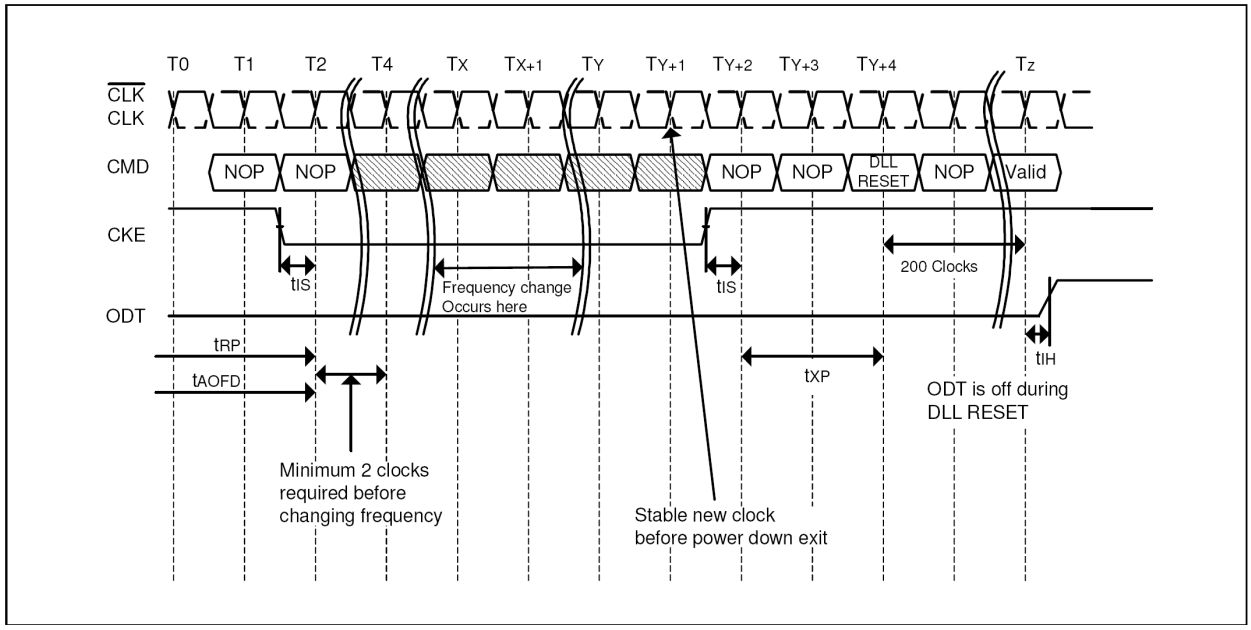
10.30. Active Power Down Mode Entry and Exit Timing



10.31. Precharged Power Down Mode Entry and Exit Timing

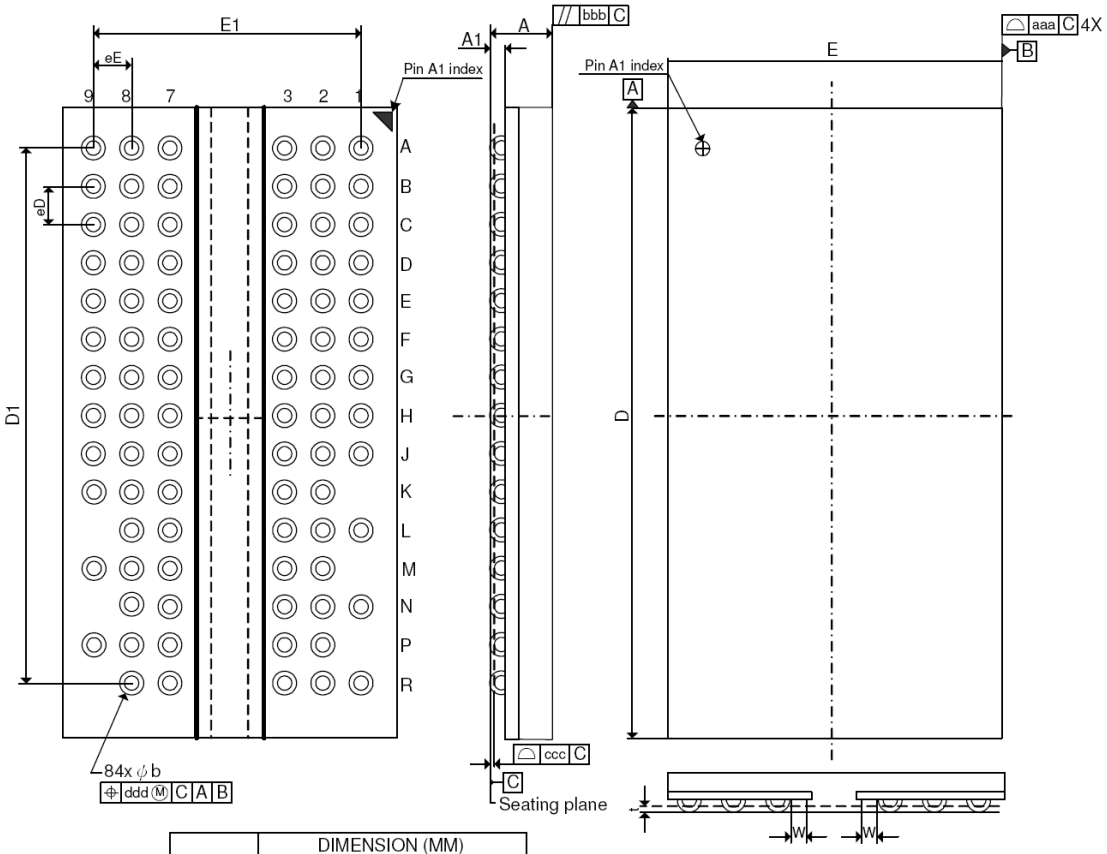


10.32. Clock frequency change in precharge Power Down mode



11. PACKAGE DRAWING

11.1. 84-ball WBGA (8x12.5 mm^2)



SYMBOL	DIMENSION (MM)		
	MIN.	NOM.	MAX.
A	---	---	1.20
A1	0.30	---	0.40
b	0.40	---	0.50
D	12.40	12.50	12.60
E	7.90	8.00	8.10
D1	11.2 BSC.		
E1	6.40 BSC.		
eE	0.80 BSC.		
eD	0.80 BSC.		
aaa	---	---	0.2
bbb	---	---	0.2
ccc	---	---	0.1
ddd	---	---	0.15
W	0.1	---	---
t	---	---	0.2

12. VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A00	2009/03/02	—	Initial Issued

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